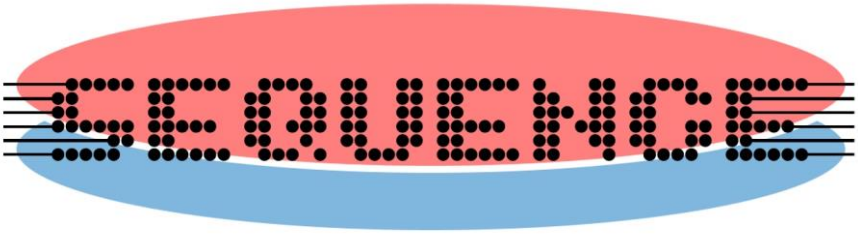
Deliverable – D4.3 Initial benchmarking towards evolving wideband communication and sensing



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Introduction

This deliverable describes state-of-the-art for transistor technology and circuitry for communication and sensing applications. The transistor data has been delivered by the SEQUENCE partners and analysed within WP2. The circuit data is selected from the literature and from the efforts within WP4. This deliverable serves as a basis for the work in the second part of SEQUENCE.

1 Device Level Benchmarking of Transistor Technologies

Four different types of transistor architectures are considered within SEQUENCE; Si SOI, Si FinFETs, III-V HEMTs and III-V MOSFETs. Combined they represent the best options for various circuit design considerations. The Si SOI and FinFET technologies provide CMOS functionality combined with integration potential for Si QuBit Devices. III-V HEMTs and III-V MOSFETs provide the best option for low noise and low-power analogue circuit building blocks critical for control and read-out electronics for Quantum applications. It is important to compare and benchmark the performance of different transistor types to be able to select the best technology option available.

During the first half of the SEQUENCE project, we have selected and benchmarked the transistor performance provided by the consortium partners and that has been measured and reported within WP2. The data is compared at two different temperatures indicated by red (RT) and blue (4K), presented in Table 1.1. During the second phase of SEQUENCE, this benchmark table will be updated and completed with data from competing efforts to compare the European effort to the international competition.

Table 1.1. Device technology benchmark comparison.

	Technology	**Company**	**L_g (nm)**	**I_{on} (µA/µm)**	**Slope**	**R_{on} Ωµm**	**g_m (mS/µm)**	**f_t/ f_{max} (GHz)**	**f_{max} (GHz)**	**V_d (V)**	**Ref**
FD-SOI	STM 28 nm	STM	30	625	75	540	1.4			0.9	[1.1]
	STM 28 nm	STM	30	625	30	466	1.7			0.9	
	GF 22 nm	GF	18		73	370	1.8			1.0	[1.2]
	GF 22 nm	GF	18		17	270	2.3			1.0	
Fin-FETs	TSMC	TSMC	16		80	237	2.5			1.1	[1.3]
	TSMC	TSMC	16		20	156	3.1			1.1	
HEMTs	30 nm mHEMT	IAF	35	-		230	2.3			0.5	[1.4]
	30 nm mHEMT	IAF				190	2.45	>500		0.5	
III-V MOS-FETs	Vertical NWs	ULUND	25			190	3.1			0.5	[1.5]

2 Digital CMOS circuits Benchmarking

Cryogenic digital CMOS design is a pioneer activity targeting the improvement of the computing performances. Even if the frozen power cost must be at the end of the day, this thematic tries to demonstrate that this approach could be a performance extension of technology nodes anterior of leading edge ones in the Moore law. We have selected two papers [2.1; 2.2] from last year presenting experiences at 77K [2.1] and at 4K [2.2]. The two temperatures can be easily achieved applying Liquid Nitrogen (LN) at 77K and Liquid Helium (LHe) at 4K. In our approach, we are targeting the CMOS optimum efficiency that would be between these two temperatures.

2.1 State of the Art Presentation

Motivation of paper [2.1] was the high performance computing cryogenic increase by a dramatic reduction of devices leakage and metallic resistance reducing the temperature, cf. Fig. 2.1. They proposed to define a specific Cryogenic architecture at 77K. They characterised and benchmarked CMOS technology-nodes over temperature showing that whatever the node, from 90nm to 180nm, the carrier mobility and the saturation velocity increase in a quasi-quadratic relation to the temperature reduction, while the threshold voltage increase linearly with the temperature reduction in the range from 300K to 77K. The drawback being the parasitic gate resistance, which increases by a factor of 20% (PMOS) and 40% (NMOS) from 300K to 77K. Finally, the On-channel current increases by 30% while the leakage current is reduced by 2 decades from 300K to 77K, cf. Fig. 2.2. In addition, they did characterisation of the metal lines, and showed that the resistivity of the metal is reduced by 2.5 times from 300K to 77K.

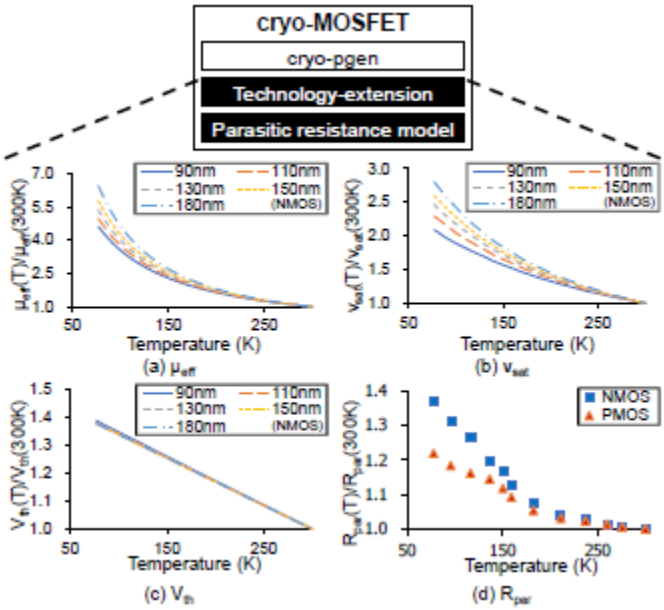

Figure 2.1. From [2.1], Extension to the baseline MOSFET model: (a) Carrier mobility; (b) Saturation velocity; (c) Threshold voltage; (d) Parasitic resistance model.

All of these parameter evolutions on actives and passives, allow them to present a high performance core (CHP-core) achieving an increase of the clock frequency by 51%, and a low power core (CLP-core) achieving a power reduction by 38% reducing temperature from 300K to 77K.

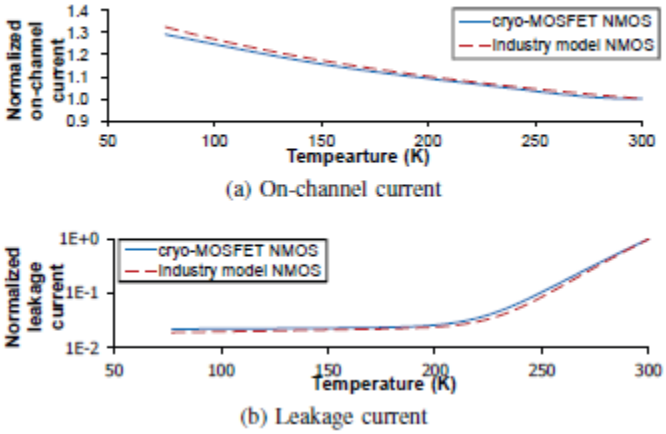

Figure 2.2. From [2.1], MOSFET Ion and Ioff versus temperature.

Motivation of paper [2.2] was the development of a RISK-V unit in CMOS 40nm, as close as possible from the Quantum qubits, this means at the lowest possible temperature, without affecting the qubit temperature, (20mK), by heating actions. They targeted 4K. The first part of the work was to do extrapolation of electrical parameter of the technology, as they did not found in the literature specific study down to 4K. Their comparison to state of the art is reproduced in Fig. 2.3. Theoretically they define a CMOS inverter VDDmin@300K = 36mV and VDDmin@4K = 2.47mV. Finally, the minimum voltage at 300K is actually 0.3V and at 4K 0.59V. This shows that extrapolations between 300K and 4K are not valid, while it was valid between 300K and 77K. Despite of this, they achieve an increase of the clock frequency at 1.2V from 475MHz at 300K to 750MHz at 4K. Finally, they concluded that the difference between theoretical values and achievable values comes from the Vth control, which is not done in Bulk CMOS, and proposes to explore in the future technologies as FDSOI, which allows the Vth control by the back-gate.

COMPARISON WITH STATE-OF-THE-ART

	This Work		ESSCIRC'18 [8]	JSSC'17 [9]
Technology	40-nm CMOS		28-nm FDSOI	40-nm CMOS
Architecture	RV32IM		RV32IM	Cortex-M0
Temperature	4.2 K	300 K	300 K	300 K
F_{MAX}	740 MHz @ 1.2 V	475 MHz @ 1.2 V	-	-
F @ V_{MIN}	9 MHz @ 0.59 V	3.2 MHz @ 0.3 V	1 MHz @ 0.25 V	0.8 MHz @ 0.2 V
Min. E_{CORE}	8.90 pJ	5.80 pJ	4.18 pJ	8.80 pJ
Min. EDP_{CORE}	0.037 pJ/MHz	0.061 pJ/MHz	0.075 pJ/MHz	0.6 pJ/MHz

Figure 2.3. From [2.2], RISK-V benchmark.

From these two experiences, we can define the trends the two research groups have exhibited. The following Table 2.1 gives a summary of these trends:

Table 2.1. Trends in frequency, power, and Vddmin for different technologies.

Papers	Circuits	Frequency trend	Power Trend	Vddmin Trend
[2.1]	CHP-core 300K to 77K 90nm-180nm Bulk	+51%	0%	-
[2.1]	CLP-core 300K to 77K 90nm-180nm Bulk	0%	-38%	-
[2.2]	RV32IM 300K to 4K 40nm Bulk	+55%	0%	+96%
[2.2]	RV32IM Meas/simu @ 4K 40nm Bulk			+23 880%

The two experiences are comparable in term of frequency increase versus the temperature; the benefit of the 4K temperature is not clear versus the one at 77K. Vddmin is the drawback of the RV32IM circuit as the Vth increases when the temperature decreases. This would be one advantage of the FDSOI process.

2.2 SEQUENCE Research Orientation

Motivation of Cryogenic Digital CMOS SEQUENCE research is:

- To fill the gap between 77K and 4K, where an optimum should be found.
- To prove the interest of FDSOI for Vth control.
- To propose new technologies in this temperature range as III-V Nanowires.

In order to evaluate the potentiality of CMOS digital structures in the 4K-77K temperature range, LETI is developing a CMOS ring oscillator in FDSOI CMOS. This structure will be characterized with and without Vth control. Without Vth control results will be comparable to [2.2] at 4K and [2.1] at 77K, in addition we should find again the trends of these two papers. With the Vth control, we will explore the advantage we would have at 4K and 77K. And we will also evaluate the models accuracy, outcomes from WP2 in the gap between 4K and 77K: Examples of tables that will be filled when measurements will be available are given in Table 2.2 and Table 2.3, now left blank.

Table 2.2. Different temperature measurements of Key parameters.

Ring-O	Parame-ters	4K	10K	30K	50K	70K	300K
Without Vth Control	Vddmin						
	Fmax						
	P @ 1.2V						
With Vth Control	Vddmin						
	Fmax						
	P @ 1.2V						

Table 2.3. Simulation / Measurement comparison on Ring-O Frequency.

Ring-O	Freq @ 1.2V	4K	10K	30K	50K	70K	300K
Without Vth Control	Meas						
	Simu						
With Vth Control	Meas						
	Simu						

The FDSOI 28nm we use are delivered by the industrial and are guaranteed down to 200K, we have done simulation of the 28nm Ring-Oscillator with and without Vth compensation by Back-gate voltage (Vbg) at this temperature, and compared to the result obtained at 300K. These results from these initial simulations are given in Table 2.4.

Table 2.4. Ring oscillator simulation results in FDSOI 28 nm.

Simulation	300K	200K with control Vbg = 0V	200K with control Vbg up to 1V
Ring-O Frequency	12,2GHz	11,7GHz	Up to 14,5GHz

This means that we can compensate the frequency variation; this result is in line with the CEA publication [2.3] where the Vth compensation of the 28nm FDSOI transistor by Vbg is presented. In these two CEA experiences, the increase of the frequency when the temperature is decreasing is not a reality as Vth increases. This is the case if maintaining Vth at the same value as at 300K.

In order to evaluate new III-V Nanowires technology at cryogenic temperature, an inverter is developed by university of Lund. This inverter will be compared to Silicon FDSOI inverter used by the Ring-oscillator developed by LETI. A comparison of the performances obtained in the best case of FDSOI to the III-V nanowires will drive the consortium to define where the technologies are the most efficient: Examples of table that will be filled when measurements will be available is given in Table 2.5, now left blank.

Table 2.5. FDSOI / III-V CMOS measurements comparison of Key parameters.

Inverter	Parame-ters	4K	10K	30K	50K	70K	300K
FDSOI	Vddmin						
	Tp						
	P @ 1.2V						
III-V Nan-owires	Vddmin						
	Tp						
	P @ 1.2V						

3 Wireless Wideband communication and sensing at Room Temperature

3.1 Multi-Frequency Signal Sources for Reference for Multi-Channel Digital Complex Modulated Communications

Multi-Qbit addressing is one of the Quantum computing applications, actually each qubit needs one manipulation connection and one read connection, the numbers of connections between ambient temperature and cryogenic temperature becomes a nightmare when increasing a lot, the number of qubits. The idea is to do multi-frequency generator which can be wired by a minimum number of connections. This is the approach we have, and in another way shown in Fig. 3.1-2, Intel approach too [3.1]. Main difference between Intel approach and ours, is the temperature where is placed the frequency generator. Intel proposes to place it close to the Qubit, at 4K, and to transfer from ambient temperature to 4K the digital control (parallel 8 bits or more). We go one step ahead, we do the multi-frequency generation at ambient temperature, and transfer only one cable with all frequencies to 4K. Between 4K and Qubit temperature, the approach is similar.

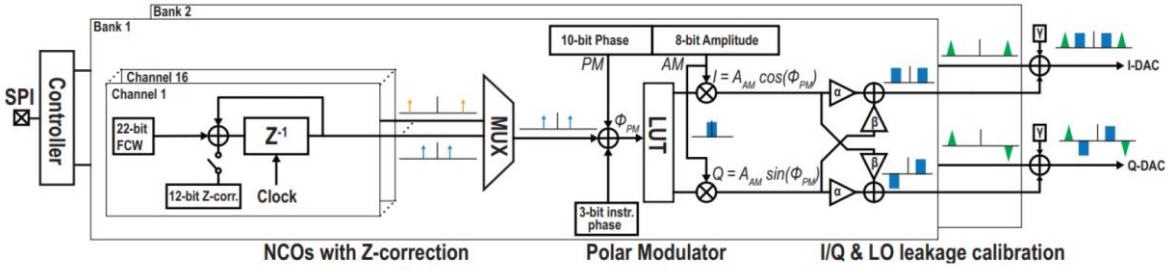

Figure 3.1. Intel approach, the circuit is in FFT 22nm and works at 4K.

		This Work	[B. Patra, 2020 ISSCC]	[J. Bardin, 2019 ISSCC]
Qubit platform		Spin qubits	Transmons + spin qubits	Transmons
Controller capability		Drive, Readout with Digital Detector, Gate Pulsing, µ-Controller	Drive	Drive
Power	Analog	Drive: 5.2mW/qubit[a] Readout TX/RX: 1.3/9.3mW/qubit Gate pulsing: 2.9mW/channel	1.7mW/qubit	<2mW/qubit
	Digital	10 – 140mW[b] @ 1.6GHz clock	Digital: 330mW @ 1GHz clock	N/A
Chip area		16mm²	4mm²	1.6mm²
Technology		22nm FinFET CMOS	22nm FinFET CMOS	28nm bulk CMOS
Drive				
Freq. range		11 – 17GHz @ >-10dBm	2 – 20GHz @ >-45dBm	4 – 8GHz
Freq. multiplexing		Yes, 16 qubits	Yes, 32 qubits	No
Sampling rate		up to 2.5GS/s	1GS/s	1GS/s
IM3		<-50dBc @ >-17dBm (11 to 17GHz)	<-50dBc @ -18dBm (6.25GHz)	N/A
Data bandwidth		up to 2GHz	1GHz	400MHz
Digital FIR		Yes, 2 notches per qubit	No	No
Envelope size		16,384 points AWG[c]	Up to 40,960 points AWG[d]	Fixed 22 points symmetric
Instruction set		2^{19} codewords per qubit	2^3 codewords per qubit	2^4 codewords
Output impedance		50Ω	N/A	N/A
LO IQ generation		Integrated on-chip hybrid	External off-chip hybrid (PCB)	External off-chip hybrid

This Work – Readout		This Work – Gate Pulsing	
Freq. multiplexing	Yes, 6 qubits	# Channels	22 (simultaneous)
TX output freq.	DC – 0.6GHz	Amplitude range	±0.4V[f]
TX output power	-70 to -40dBm	Amplitude res.	11 bits
RX RF freq.	200 – 600MHz	Pulse width	10ns – 2.6ms
RX gain	40 – 90dB	Pulse width resolution	2.5ns
RX noise temperature[e]	44K	Rise/fall time	~50ns[g]
RX baseband BW	60 – 200MHz	Output rms noise	200µV_{rms}
Filter order	8th	Output impedance	50Ω
ADC	SAR, 7.5 bits, 400MS/s		
Qubit state detector	Integrated		

[a]For max P_{out}
[b]Depending on activity
[c]Per codeword, per qubit
[d]Shared for 8 codewords and 16 qubits
[e]Integrated over 60MHz BW
[f]Around DC output voltage
[g]With 14pF load

Figure 3.2. Intel work compared to the previous state of Art.

We will compare our approach to these ones, the first point, is that we don't work at 4K, then we don't have Thermic issues, as they have in their approaches. Second point, in this demonstration we have limited our band to 6GHz with frequency step of 1GHz, but the concept can be extended to bigger bands, with bigger number of steps. For this first benchmark, we don't have measurement results, the foundry step begins end of June 21, we will have results beginning of 2022.

3.2 Wideband D-band RF-Switches

In Table 3.1 various technologies of primarily λ/4-shunt SPDT switches for D-band are benchmarked Different technologies with similar topologies are compared to understand state of the art performance for D-band switches. Wideband D-band switches are a necessity in different kind of high frequency systems such as communication systems, radars, and remote sensing. The technologies that are considered within the SEQUENCE project are promising for usage within these applications. Initial benchmarking of SPDT D-band switches is reported in this section.

Table 3.1. Benchmark of SPDT switches.

Ref.	Technology	Topology	First author affiliation	f_T/f_{MAX} (GHz)	Year	freq (GHz)	Insertion loss(dB)	Isolation (dB)	$r_{on}\cdot C_{off}$ (fs)	Comment
[3.2]	32nm CMOS SOI	λ/4-shunt	Georgia Institute of Technology	210/245	2015	110-170	2.6-4	22	-	
[3.3]	50nm InGaAs mHEMT	λ/4-shunt	Fraunhofer (IAF)	375/670	2018	52-168	3.1	42.1	110.3	
[3.3]	50nm InGaAs mHEMT	Novel λ/4-shunt	Fraunhofer (IAF)	375/670	2018	75-170	4.5	56.4	110.3	
[3.4]	0.13 um SiGe HBT	λ/4-shunt	Georgia Institute of Technology	300/500	2014	96-163	2.6-3	23.5-29	83.7	
[3.5]	0.13 um SiGe HBT	λ/4-shunt	IHP	300/500	2019	110-170	2.0-3.0	21-26	-	
[3.6]	800 nm InP DHBT	λ/4-shunt	Ferdinand-Braun-Institut (FBH)	350/350	2019	90-170	3.0-5.0	42-55	-	
[3.7]	65 nm CMOS	λ/4-shunt	University of Toronto	300/400	2009	110-170	4.0-5.0	26.5-32	-	
[3.8]	0.13 µm SiGe BiCMOS	RF MEMS	IHP	505/720	2017	110-170	1.42-1.9	20-54.5	-	
[3.9]	50nm InGaAs NW*	λ/4-shunt	Lund University	-/-	2020	29-69	2.7	27.2	165	
[3.10]	50 nm InGaAs NW*	λ/4-shunt	C2Amps + Lund University	310/350	2020	97.5-120	2	>20	-	
This Work	50nm, InGaAs NW *	λ/4-shunt	C2Amps	310/350	2021	110-170	2.65	>20	135	

*Simulated

The switch performance as well as the technology f_T/f_{max} is reported. Isolation and insertion loss demands vary between applications. Generally, in a transceiver the antenna switch will switch between the antenna and LNA while the PA always is connected to the antenna. It is not feasible to have the insertion loss from a switch in series with the PA because the loss would be too large. The switch insertion loss will need to be as low as possible to keep the noise figure of the receiver low. Isolation will need to be sufficient so that the output signal of the PA does not break the LNA. In mm-Wave systems the output power of the PA is lower than for systems for lower frequencies (4G around 26dB and 5G around 15 dBm). The isolation requirement should follow the same trend and is then lower than previously.

State of the art performance is around 2-2.5 dB insertion loss and around 25 dB isolation for the standard λ/4-shunt topology, novel topologies can reach isolation up to 55 dB.

The reported values for vertical nanowire switches are simulated results only, however the results show great promise especially considering the Ft/Fmax of the technology. There is great reason to look further into using the nanowire technology for high frequency band switches. Manufacturing of vertical nanowire switches is scheduled within the SEQUENCE project.

3.3 Integration of LNAs and RF-Switches

The D-band LNA benchmark is provided in Table 3.2. In general, for an LNA, regardless of carrier frequency, the most important performance metrics are the noise figure (NF), gain, linearity, and compression point. For validation of millimeter wave LNAs, there is often only one signal generator available, therefore, intermodulation measurements are often missing. A large bandwidth is desirable, since it makes the LNA more resilient to process spread. A high gain can be achieved by cascading several stages, at the prize of increased power consumption. The noise figure is to a large extent impacted by the f_T/f_{MAX} of the process technology. If the carrier frequency is too close to the cut-off frequency, the NF will deteriorate strongly. However, the back end of line (BEOL) of the process technology also has a significant impact, due to the limited Q-value of inductors and transformers. When comparing different LNAs it is important to distinguish between wafer and packages measurements. A commercial standalone LNA always includes a package that can add around 1 dB loss at D-band frequencies. In the table, GaAs mHEMT, CMOS, GaN, InP DHBT, InP HEMT, SiGe, and Vertical Nanowire (VNW) designs are compared. For the InP HEMT, GaN DHFET and VNW designs, only simulated data is reported. The VNW device has the lowest NF of 2.8 dB (simulated), while the highest reported NF is at about 6 dB (GaN DHFET projected only). The GaInAs mHEMT from Fraunhofer has the lowest measured NF of 3.0 dB. An LNA designed in a quite old technology (CMOS 65) has a measured NF of 4.7 dB @148 GHz. The bandwidth of that design is only 11 GHz though. The VNW design also suffers from low BW (10 GHz).

Table 3.2. Benchmark of D-band LNAs.

Ref.	Technology	Topology	First author affiliation	f_T/f_{MAX} (GHz)	Year	Max S21 (dB)	BW_{3dB} (GHz)	Min NF (dB)	VCC (V)	P_{DC} (mW)	Comment
[3.11]	GaAs 40 nm mHEMT	4 stages	University of Rome	400/600	2017	>20	115-160	4.0 @140 GHz	1.2	82	OMMIC foundry in France
[3.12]	GaInAs mHEMT 50 nm	Casc, Casc, Casc	Fraunhofer	380/670	2017	30.8	97-155	3.0 dB @119 GHz 3.4 (mean)	1.4	57.6	
[3.13]	CMOS 65 nm	SE, 2 CS	KAIST, Korea	/310	2021	17.9	11	4.7 @148 GHz, 6.2 @150 GHz	0.65	13.73	Advanced matching network, narrowband
[3.14]	GaN DHFET T-gate 40 nm	SE, 6 stages	HRL laboratories, Malibu	200/400	2017	>25	110-170	~6 (projected)	5	225	NF not measured
[3.15]	InP DHBT	Single device	Brandenburg univ.	330/350	2020	-	-	6.0 @105 GHz	1.5	7.5	Device measurement, W-band, wafer
[3.16]	InP HEMT	5 CS	Hangzhou Dianzi University, Hangzhou, China	-	2018	>18.5	120-150	<4.5	-	47	Simulation only, wafer
[3.17]	SiGe 0.13 µm BiCMOS	CS, Casc, Casc, Cs	Sabanci Univ, Turkey, IHP	300/500	2018	25.3	112-156	5.9 (fitted)	1.5/2.5	30	Wafer
[3.18]	SiGe 0.13 µm BiCMOS	Casc, Casc	Georgia Institute of Technology	300/500	2015	>20	110-140	5.5	2.0	112	Inductive CB base termination
[3.19]	SiGe 0.13 µm BiCMOS	4 Casc	Sabanci Univ, Turkey, IHP	300/500	2018	32.6	52	4.8	-	28	NF <6.1dB across D-band
[3.10]	50 nm InGaAs NW*	Diff, Casc, Casc	C2Amps + Lund University	310/350	2020	24.5	10	2.8	1.5/2.5	73.1	Simulated only

4 Wireless Space 40K - 70K communications and sensing

4.1 Quadrature LO signals for the RX and TX chains (E-band at RT)

The direct-conversion transceiver architecture with zero-IF does not require any external filter. This means high integration level and low cost. However, the LO frequency is equal to the center frequency of the RF signal. This could result in issues with self-mixing in the receiver as well as LO pulling at the transmitter. A subharmonic mixer (SHM) typically utilizes the second-order harmonic of the mixer, thereby solving the issues above.

4.1.1 LO signal architectures-sub-harmonic generation

A subharmonic mixer [4.1]-[4.8] often uses the second order nonlinearity (2x SHM) of the mixer core. However, 3x SHMs [4.1] and 4xSHMs have also been designed. The mixing element could also be a Schottky diode. Yet another alternative is to create a LO signal that is rich in second order harmonics

(LO signal with 25% duty cycle) [4.4]. This is however not really an alternative at mm-wave frequencies. A benchmark of sub-harmonic mixers is provided in Table 4.1. The diode-based SHMs usually have quite low gain, increasing the requirements on the preceding LNA. The SHMs based on active mixers have higher gain. An advantage is that the frequency of the VCO is reduced, thereby improving the phase noise. The referenced works do not have a PLL included.

Table 4.1. Sub-harmonic LO generation benchmark.

Ref.	Technology	Topology	PLL included	First author affiliation	f_T/f_{MAX} (GHz)	Year	Max G_{conv} (dB)	freq. (GHz)	OP_{1dB} (dBm)	Isol. 2LO-RF (dB)	P_{DC} (mW)	Comment
[4.2]	0.13 µm SiGe BiCMOS with	2xSHM, active mixer	No	MC2, Chalmers	250/370	2017	2.6	98-140	-6	45	46	Switching mixer core in fundamental tone, LO doubling in tail.
[4.3]	Discrete, Skyworks Schottky diodes DMK2308	4xSHM, diode	No	Lahore, Pakistan	-	2015	-13.4	57-59	-	>50	N/A	Simulated
[4.5]	GaAs 70nm mHEMT	2x SHM, Coupler, diode	No	Hangzhou, China	-	2020	-16.2	110-170	-	In the meas. Noise floor	13.73	Broadband
[4.6]	CMOS 90 nm	2x SHM, active mixer	No	Taiwan univ.	-	2018	9	70-88	-	>40	5	High conversion gain, low PDC
[4.7]	0.13 µm pHEMT	2x SHM, diode	No	Plextek, UK	-	2012	-11	71-86	-	-	-	
[4.8]	CMOS 65nm	2xSHM, mixer	No	Kaist, Korea	-	2015	3.4	75-81	-15.6	38	12	Gm-boost

4.1.2 LO signal architectures-harmonic generation (no sub. harm. Mixer)

An LO architecture based on harmonic signal generation [4.9]-[4.14] is based around a VCO (or QVCO) that is at a fraction of the wanted carrier frequency. The upconversion to carrier LO frequency is not based on for instance the second order nonlinearity of the mixer core as for the sub-harmonic mixer, and the conversion gain is therefore higher. A benchmark of harmonic LO generation is provided in Table 4.2. For frequency multiplication, techniques such as injection locking, harmonic tripler circuits and upconversion active mixers can be used. The architectures are generally less complex than the ones used in the SHMs. Generally, at mm-wave frequencies, architectures that are based on polyphase filters for creation of different LO phases should be avoided, since the matching and process spread becomes worse with increasing frequency. Phase mismatch is also an issue for the QVCO in the selected topology. A competitive PLL should typically have a phase noise that is less than -90 dBc/Hz @ 1 MHz offset. The actual system requirement depends on the modulation scheme and the application. Typically, fixed radio links do not change their carrier frequency so PLL locking time is less of an issue. The PLL bandwidth can therefore be set low, which suppresses the phase noise of the VCO inside the loop bandwidth.

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Table 4.2. Harmonic LO generation benchmark.

Ref	Technology	Topology	With PLL	First author affiliation	f_T/f_{MAX} (GHz)	Year	PN (dBc/Hz @ 1MHz offset)	freq. (GHz)	P_{DC} (mW)	Comment
[4.9]	SiGe 0.18 µm BiCMOS	30 GHz PLL plus triplers	Yes	UCLA, USA	200/180	2012	-93 @96 GHz	90.9-101.4	140	Based on frequency triplers
[4.10]	CMOS 65 nm	Injection locked QVCO (QILO) QILO is used as a frequency tripler.	Yes	Tokyo, Inst. Of Tech.	-	2011	-95 @60 GHz	58-63	80	20 GHz PLL
[4.11]	IBM CMOS 130 nm	Triple push VCO	No	Rensselaer Polytechnic Institute, USA	-	2010	-95 @ 10 MHz offset	55-65	95	Three VCO's @ 20 GHz
[4.12]	CMOS 65 nm	Doubler, IQ div., inj. locked tripler	Yes	Hong Kong Univ.	-	2015	-92	59-86	54	
[4.13]	SiGe 0.18 µm	Sliding IF	No	Lund Univ.	200/250	2016	-97.5 (est.)	81-86	109	Including QVCO and upconverter
[4.14]	SiGe 0.18 µm	QVCO + active loop filter	Yes, only PLL no LO at carrier freq.	Lund Univ.	200/250	2016	-107 @28 GHz	28	56.7	Based on 28 GHz QVCO, corresponds to -97.5 dBc/Hz @84 GHz

4.1.3 Conclusions LO generation in RT

Several options are available for LO generation for E-band mixers. However, the LO generation cannot be analyzed standalone. Instead, the performance of e.g. the mixer also sets the requirements on the surrounding blocks like the RX LNA. If there is significant attenuation in the mixer, the LNA will need to provide more gain to overcome the noise of the mixer.

It is advantageous to base the LO generation on a VCO that operates on a fraction of the LO-frequency since this improves the phase noise and reduces the power consumption of the VCO.

At mm-wave frequencies, the effect of capacitance mismatch becomes more severe, and it is difficult to control the phase of LO signal with accuracy. Architectures based on cancellation of unwanted harmonics by adding LO signals with different phases in subharmonic mixers are therefore less suitable. The use of polyphase filters for generating the required LO phases for subharmonic mixers cannot be recommended unless mismatch can be controlled.

A SHM always has lower gain for the harmonics than the fundamental. A passive SHM can be designed using anti-parallel Schottky diodes. These can be used in e.g. 2x or 4x SHM:s. It is a simple design, but a large drawback is the low conversion gain, often lower than -10 dB.

A low complexity of the LO generation is always desired. If the layout becomes complicated and matching is crucial, it is less probable to be successful without several iterations. **The selected topology for E-band LO generation is the sliding IF architecture based on a VCO that is the LO-frequency divided by three**.

Compared to the SHM presented in [4.1], the VCO frequency could be selected to be the same as in the selected topology. In the sliding IF-architecture, the design is based on a QVC0, which is a slightly more complex topology. However, the active mixers in the selected topology operate on their fundamental LO frequency, thereby generating a substantial gain. With $f_{QVCO} = f_{LO}/3$ there is significantly less pulling of the VCO from PA in a transmitter.

A drawback is the more complex layout since both the four fundamental signals at 28 GHz and the second harmonic at 56 GHz need to be routed out from the QVCO without interfering with each other. A second drawback is the power consumption of the driver buffers for the 28 and 56 GHz LO signals.This topology does not depend on cancellation of unwanted harmonics created in the SHM in [4.1]. This is a large advantage.

4.2 Benchmarking of E/W-Band LNA + Switch

State-of-the-art LNAs in the frequency range from of approximately 70 – 116 GHz are based on InGaAs HEMT devices and are made either of so called InP HEMTs or metamorphic HEMTs (mHEMTs). Reported data in literature either target applications with room temperature or in the temperature range of approximately 15 K. In the temperature range of approximately 40 – 70 K no noise temperature can be found. However, the temperature range of around 50 K is most interesting for future satellite sensing applications, e.g. weather observation satellites. Technology improvements over the past years improved the system noise temperature of such systems down to a limit where further performance improvements at room temperature are more and more difficult to achieve.

Since noise measurement setup at cryogenic conditions in the frequency range of around 100 GHz in general do not allow on-wafer probing, noise measurements under these conditions require the packaging of the LNA MMICs in waveguide housings. One has to be kept in mind that the packaging cause additional loss, which are then part of the measured noise temperature of such LNAs. Thus, all LNAs in the given list are LNA modules. Corresponding state-of-the-art results including the simulated results, which are reported in D4.2, are given in Table 4.3. For room temperature condition, the listed data in Table 4.4 are MMIC results. This allows a better comparison to the simulated data of D4.2.

Table 4.3: State-of-the-Art E/W-Band LNA Modules Operating at Cryogenic Conditions.

Reference	Technology	Frequency [GHz]	Ambient Temperature [K]	Gain [dB]	Noise Temperature [K]
[4.15]	50-nm InGaAs mHEMT	70 – 116	15	21.8 – 27.7	20.6 – 40.1
[4.15]	35-nm InGaAs mHEMT	70 – 116	15	19.1 – 28	23 – 41.9
[4.16]	35-nm InP HEMT	70 – 114	20	< 15	22 – 28
[4.17]	35-nm InP HEMT	75 – 116	27	20 – 29	25 – 39
[4.18]	35-nm InP HEMT	75 – 115	22	23 – 32	24 – 41
[4.19]	35-nm InP HEMT	85 – 116	27	20 – 29	23 – 33
[4.20]	100-nm InP HEMT	65 – 116	16	n/a	22.3 – 40
This work D4.2	50-nm InGaAs mHEMT	min. 75 – 110	50	26 – 29	31.2 – 38.2

Table 4.4. State-of-the-Art E/W-Band LNA MMICs Operating at Room Temperature.

Reference	Technology	Frequency [GHz]	Gain [dB]	Noise Temperature [K]
[4.21]	35-nm InGaAs mHEMT	75 – 110	23 – 28	129 – 191 (avg. 159)
[4.22]	50-nm InGaAs mHEMT	75 – 108	25 – 33	132 – 243 (avg. 159)
[4.23]	50-nm InGaAs mHEMT	71 – 86	20 – 26	129 – 202 (avg. 159)
[4.24]	50-nm InGaAs mHEMT	66 – 104	20 – 27	139 – 226
[4.21]	50-nm InGaAs mHEMT	75 – 110	20 – 27	149 – 238 (avg. 180)
[4.25]	35-nm InP HEMT	75 – 90	22.5 – 29	129 – 226
This work D4.2	50-nm InGaAs mHEMT	min. 75 – 110	25 – 29	130 – 159

For SPDT switch MMICs in the W-band frequency range, literature values are only available for room temperature operation. Thus, Table 4.5 shows only room-temperature data.

Table 4.5 State-of-the-Art E/W-Band Switch MMICs Operating at Room Temperature.

Reference	Technology	Frequency [GHz]	Isolation [dB]	Insertion Loss [dB]
[4.26]	50-nm InGaAs mHEMT	75 – 110	28.5 – 31.4	1 – 1.6
[4.27]	InGaAs pHEMT	50 – 70	32 – 41.3	1.3 – 1.8
[4.28]	GaAs pHEMT	40 – 85	> 31	1.2 – 2
[4.29]	100-nm GaN HEMT	60 – 90	22.5 – 25.5	1.5 – 1.8
[4.30]	GaAs Diode	75 – 110	> 31	1.1 – 1.6
[4.31]	100-nm GaN HEMT	72 – 131	18.5 – 21.5	1.1 – 2
[4.32]	SiGe Diode	77 – 133	19 – 22	1.4 – 2
[4.33]	50-nm InGaAs mHEMT	143 – 305	13.5 – 22.8	1.5 – 2.5
This work D4.2 297 K 50 K	50-nm InGaAs mHEMT	 min. 75 – 110 min. 75 – 110	 > 30 > 30	 1 – 1.4 0.8 – 1.1

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