Deliverable – D4.1 Review of key building blocks for cryogenic logic and space, 40-70 K, as well as wideband communication, RT

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1 Introduction

The Cryogenic Technology Platform developed in SEQUENCE is mainly aimed to serve Quantum computing applications, bringing control and sense electronics as close as possible to the Qubits, this means close to zero-degree Kelvin. In addition, such a Cryogenic Technology Platform can serve others markets, increasing the field of application domains. The first question mark is what are the specifications of this technology platform at the very low operation temperature? Actually, the majority of the technologies studied in SEQUENCE have

the capacity to address mmW frequency applications, while some can address high speed digital or ultra-low power applications. These technologies in general, are well defined to address communication, sensing, and computing applications. In this way, we have defined three domains, apart from quantum technologies, where the Cryogenic Technology Platform is efficient.

- **Wireless space 40K – 70K communications and sensing** are using the mmW frequency range, where cooling the receiver functions can increase the sensibility for the sensing applications, and can increase the signal over noise ratio for communications applications.
- **Logic Building blocks used in the 40K – 70K** range should be at their maximum efficiency, which opens the High-performance computing applications field. In addition, some of the technologies developed in SEQUENCE can bring improvements for applications at room temperature e.g. reduce the power consumption of edge computing functions in the IoT applications field.
- **Wireless Wideband communication and sensing**, at Room Temperature, defined in mmW frequency range, profit from the High frequency specifications of the technologies developed in this project, to open doors to beyond 5G to 6G.

These three application domains are introduced in this deliverable, and circuits proposed in each domain will bring proof of concept of the capacity to use the Cryogenic Technology Platform in these different application fields, increasing the exploitation perspective of the platform.

2 Wireless Space 40K - 70K communications and sensing

2.1 Introduction

Space services are a fundamental need in our modern society. Weather forecast services and climate models rely on observation data made by satellites. Therefore, specific resonance frequencies of molecules in the atmosphere are observed with satellite-based highly-sensitive receiver systems. A major development in this field is, for instance, the Meteorological Operational Satellite - Second Generation “MetOp-SG” of the European Space Agency (ESA). The satellites will contain several receiver systems, such as, a Microwave Sounder, a Microwave Imager, or an Ice Cloud Imager with observation frequencies at, e.g., 54, 89, 118, 165, 183, 229, 243 GHz.

Furthermore, wireless satellite communication faces an increasing demand of high data rate links space to earth and space to space. Therefore, the ITU allocated frequency bands from 71-76 GHz (downlink) and 81-86 GHz (uplink) for satellite communication. In addition to established satellite platforms, new approaches, such as, “NewSpace” push into the market and further facilitate new concepts and topologies for satellite systems.

The WP4 partners, involved in Task 4.2, propose to evaluate specific building blocks that gain from a cryogenic technology platform in the 40 – 70 Kelvin range, for wireless space communication and sensing.

2.1.1. Future Challenges for Satellite-Based Sensing and Communication

During the past years, semiconductor technologies heavily evolved so that a further improvement of the receiver sensitivity of room-temperature-based satellite systems seems only possible in a marginal range. Especially for satellite-based sensing applications, the receiver sensitivity or signal-to-noise ratio is an important measure since weak signals have to be detected. Also, for satellite communication, from a system point of view, an improved receiver sensitivity is of a major interest since the output power that can be efficiently generated, e.g. in the satellite, is limited – especially at high frequencies, such as the 71-76 GHz and 81-86 GHz range. Thus, cooled receiver approaches are an appealing opportunity for further improving the

sensitivity of receiver systems and by that the resolution in sensing applications or the link budget in a communication scenario. In the meantime, cooling systems in the 40 – 70 Kelvin range are available that allow for a usage in satellites which makes this temperature range very attractive for such applications.

2.1.2. The SEQUENCE Approach to These Challenges

Technology platforms and insights of circuits and device design can facilitate the developments in this area of application. Thereby, this task can benefit from developments made in WP1 and WP3. Even though if the technology platforms, developed in WP1, mainly target ambient temperatures in the lower Kelvin range and even below, the fundamental improvements also enable improvements in the 40-70 Kelvin range. Therefore, Task 4.2 will investigate the following building blocks.

2.2 Building Blocks Description

2.2.1. Critical Components and Architectures

From a system point of view, the section of a satellite that benefit most from an ambient temperature in the range of 40-70 Kelvin is the receiver system, specifically its signal-to-noise ratio. Since the low-noise amplifier (LNA) is one of the major components in a receiver, it gains the most from the improved noise performance. Since, due to Friis' law, losses before the first LNA directly impact the receiver noise figure, building blocks in front of the LNA are equally important. Thus, RF switches which are required for calibration in a radiometer approach and possibly also in a wireless space communications case benefit as well from a reduced ambient temperature. The noise contribution of components subsequent to the LNA are suppressed by the LNA gain. Thus, it is only of a minor importance to cool, e.g., the mixer of a receiver.

To complete this study, an exploration will be done on frequency synthesizer functions, in order to evaluate the potential impact of temperature on the parameters listed below:

- Phase noise
- I/Q Balance
- Power consumption
- Frequency range
- Complexity
- Spurious emission

This work is based on an initial study made on suitable architectures for quadrature signal generation for E-Band applications. For a mmW transceiver, the best suited architecture for LO generation depends on operating frequency, the semiconductor device performance and the radio system requirements. The key active device performance is the high frequency gain, the nonlinearities and the noise. The most important parameters for the passive devices are the Q-values for the inductors, capacitors and varactors. Since the I/Q balance of the LO signals is quite important, it is important to have a sufficiently good matching for both the active and passive devices. On a radio system level, the performance of the devices in the LO chain will limit the Error Vector Magnitude (EVM) of the transceiver. In mobile terminals operating at around 2 GHz, it is common to use so called direct conversion where the PLL is locked at the carrier frequency and a quadrature voltage-controlled oscillator (QVCO) is used to generate the four LO phases. However, for a mm-wave transceiver this topology has drawbacks. It is difficult to design a QVCO at such a high frequency due to the generally poor phase noise of the varactors and the phase and amplitude mismatch of the four QVCO signals increases the frequency. An alternative would be to choose an architecture with a VCO at two times the carrier frequency followed by an I/Q divider, but this is not recommended.

Other published studied topologies are based on tripler circuits, i.e. the PLL is locked at one third of the carrier frequency and injection locked or harmonic-based frequency triplers are used to generate the LO signals at the carrier frequency. However, tripler circuits do consume a lot of power and are known to generate spurs.

Considering the above key metrics, a sliding IF TX architecture, depicted below, is recommended for more detailed studies using III-V vertical nanowire transistor models.

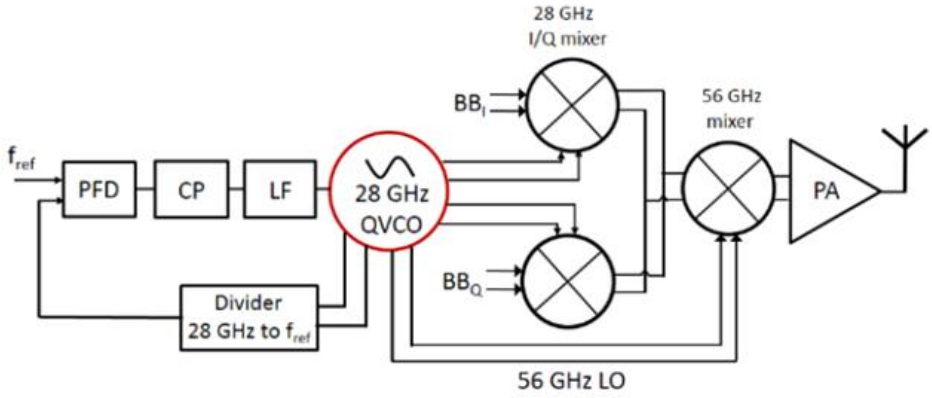

Figure 1: Sliding IF Architecture

The architecture is based on QVCO operating at one third of the carrier frequency. Operating the QVCO at this frequency improves the phase noise, tuning range and I/Q imbalance. The baseband signal is first upconverted by the 28 GHz I/Q mixers. The 56 GHz second harmonic present at the source terminal of the QVCO devices is then used to upconvert the signal to 84 GHz in a second mixer. No frequency doublers are required. One drawback is that the layout will be more complex, since, a third mixer is required.

The Sliding IF TX architecture is recommended considering the above key metrics, an exploration will be done in Task 4.2 by CTA in order to evaluate the benefit in phase noise at cryogenic temperature, this structure is adapted for E-Band communication in satellite application. CTA will evaluate the III-V nanowire process developed by ULUND, this will enrich the number of technologies that can serve satellite 40-70K applications.

2.2.2. HEMT/MOSHEMT Technologies for Receiver Applications

HEMT technologies that are based on a high-indium-content InGaAs channel are known for state-of-the-art noise performance at room temperature as well as cryogenic temperatures. Thus, the main technology that will be used for the evaluation for receiver applications at the 40 – 70 K range for an improved signal-to-noise ratio is a 50-nm gate-length metamorphic HEMT technology. One of the major research interests is how much of the noise improvement going down to the 4-K ambient class can be achieved by cooling down to the 40-70 Kelvin range. In addition, novel MOSHEMT technologies, having the benefit of severely reduced gate leakage currents, are promising candidates. Therefore, an evaluation of the MOSHEMT will be done on simulation level and, at least, by means of fabricated essential building blocks.

2.2.3. Building Blocks to Evaluate the Synergies with Technologies for Quantum Computing

- LNAs in the E-band frequency range with an intended improvement of the noise temperature by a factor of four, compared to room temperature. The targeted technology is 50 nm mHEMT and, at least, investigations based on simulations with MOSHEMT
- RF switches (SPDT) for use in radiometer applications (for calibration purposes)
- A Sliding IF TX architecture for E-Band communication

3 Logic Building Blocks for 40K - 70K

3.1 Introduction

The Electronics Components and Systems Strategic Research Agenda (ECS-SRA) underlines the need of an European independent technology platform for High Performance Computing (HPC), and edge AI. The cryogenic technology platform, under development in SEQUENCE, aim to cover Quantum Computing needs at temperatures close to zero Kelvin, but can also bring solutions for classic logic computing at higher temperatures, in the range of 40 – 70 Kelvin, and at room temperature. The technologies presented in SEQUENCE: Fully Depleted SOI CMOS, InGaAs Nanowires on silicon, and Tunnel FETs should present an optimum speed in the temperature range 40 – 70K for HPC, and at room temperature for Edge computing. The WP4 partners, involved in Task 4.3, will evaluate the efficiency benefit working with the cryogenic technology platform in 40 – 70 Kelvin range through specific building blocks for HPC and room temperature for edge AI.

3.2 Electronics Components and Systems Strategic Research Agenda Computing highlights

3.2.1. ECS-SRA 2019

The hardware and architecture challenges: Next generation hardware faces a huge challenge: **an increase by a factor of at least 50 in performance to be combined with technology breakthroughs to reduce the power consumption by a factor of 100.** For example, an extrapolation of the power load using current technology will require over a gigawatt for future exascale systems. The technical axes of exploration for power reduction, in hardware design, include:

- Energy efficient building blocks (CPU, memory, reducing length of interconnects) possibly based on 3D silicon technologies;
- Extensive usage of accelerated computing technologies (e.g. GPU, FPGA) to complement general-purpose processor;
- Reduction of the communication cost between storage and computing (computing near memory, if not in memory);
- Domain specific integration (System in Package, System on Chip);
- Domain specific customized accelerators (e.g. for deep-learning, cryptography, …);
- Integrated photonic backplane;
- Cooling and packaging technologies, etc.

This challenge is recognized by Europe that launched a "**Framework Partnership Agreement in European low-power microprocessor technologies**" (call ICT-42-2017 closed on September 26, 2017), but the effort needs to continue.

3.2.2. ECS-SRA 2020

Computing and storage now tend to form a continuum between extreme edge devices, edge devices, IoT, Fog, Cloud and HPC. Applications are increasingly distributed, and computing and storage have to be placed where they are most efficient. This trend is observed through the edge intelligence (aka Cognitive CPS, Intelligent Embedded Systems, Autonomous CPS) where data is transformed into information as early as possible to ensure privacy, efficiency and safety requirements. Having intelligent processing at the edge has pushed forward the requirement for computing and storage to be even more energy efficient and affordable. This trend leads to the following major challenges for computing technologies:

- Increasing performance (including efficiency) at acceptable costs

- High Performance Computing (HPC) and servers,
- Data Analytics (data-intensive systems) and High-Throughput Systems (HTC),
- Low power and ultra-low power intelligent computing (edge and deep edge computing).

3.3 The SEQUENCE Approach to These Challenges

In Task 4.3 dedicated to logic building blocks, the SEQUENCE technology platform will explore, silicon-based technologies, such as, Fully Depleted SOI CMOS, InGaAs Nanowire FETs, and Tunnel FET process in the mK to Room temperature range. These technologies will be evaluated to improve efficiency, either for High Performance Computing or Edge computing.

High Performance computing is mainly centralized in Data centers and computer farms. The centralization of all the computing means in one localization simplifies the cooling if it is needed. The main reason to cool computers is that CMOS Logic has an optimum efficiency in the range of 40-70K, where F_T, and g_m are maximized due to parasitic resistance reduction. Below 40K, it seems that carrier's mobility decreases. We will try to find this optimum temperature for the different technologies used in the cryogenic platform. Either in a classic CMOS logic architecture or in the Coupled Mode Logic architecture.

Edge computing, (Edge AI), is dedicated to sensor networks operating with drastic power constraints. Since such sensors are abundant and distributed, cooling is not an option. Instead, the programmable power consumed versus sensor activity is the trade-off to optimize. FDSOI silicon CMOS processes offer the opportunity to modulate the threshold voltage (V_t) of the FET transistor by the backbias, modifying the drive current of the transistor which alters its power consumption and speed. This approach will be explored to adapt the power consumption dynamically depending on the varying need. In addition, Tunnel FET transistors developed for the cryogenic platform, dramatically decrease the required supply voltage, which would drastically improve the power consumption of isolated sensors needed for specific embedded AI. The consortium will follow this second exploration track.

In a Summary, SEQUENCE technology platform can bring the following benefits for HPC and Edge computing (Edge AI) applications:

- Low temperature – Ultra low temperature optimized power consumption by operation: through the optimization of speed versus temperature. (HPC)
- High-speed logic at cryogenic temperature: through Coupled Mode Logic. (CML)
- High data rate µm to cm size connectivity: through adapted mmW to THz communications, (HPC, treated in paragraph 4)
- Programmable Power / activity: through the FDSOI back gate V_t control. (HPC @ 40-70 K & Edge AI & Room Temperature)
- High Efficient ultra-low voltage logic: for IoT computing at Room Temperature (Edge AI).

3.4 Building Blocks Description

3.4.1. Technologies to be Explored

- FDSOI process: The consortium will exploit the back-gate Threshold voltage modulation capability. This is a unique feature of such FDSOI technologies, which could address highly efficient logic building blocks, and high-speed digital applications.
- Tunnel FET process: Low V_t combined with low V_{sat} of the transistors allow development of very low supply voltage logic and analog building blocks.
- III-V nanowire FETs: The consortium will exploit the high speed at low temperature operation of this process for very high-speed digital applications.

3.4.2. Logic and Analog Architectures for HPC or Edge Computing AI Applications

- CMOS logic needs both N-MOSFET and P-MOSFET technologies, both for the FDSOI and the III-V nanowire MOSFETs. Tunnel FET transistors are N-FET transistors, evaluation of their integration with a P-MOSFETs will be done.
- CML can be done only with N-MOSFET transistors, the inverter architecture being a differential pair with a current source, (consisting of one N-MOS), and two “resistors”, (consisting also of N-MOS). Each explored technology presented above presents the possibility to do a N-FET CML inverter structures.
- Differential pairs are the most analog functions, they will be able to act as a buffer, (with resistors and current source), trans-impedance amplifiers, (buffer with resistor feedback and current sink), current reference (with current source and mirror transistors), bandgap structures (more complex combination of current/voltage references and mirror transistors), and so on.

3.4.3. Block for the Evaluation of the Cryogenic Platform for HPC and Edge AI

- CML circuits including inverters and latches will deliver information about speed and drivability and will be suitable building blocks to evaluate the performance of emerging technologies like III-V nanowire MOSFETs.
- The Ring Oscillators will deliver information on the Logic speed, and F_T, this structure is interesting as it would give the optimum speed versus temperature curve, in addition, playing with the V_T control, in FDSOI process, we will be able to evaluate the variation of the optimum speed for different V_T.
- The DFF structure, when included in a scrambler architecture would deliver information on the set and Hold time, and the rising/falling ramps through Eye Diagram measurements. This is also an exploration track to be exploited for each technology presented in this chapter.
- The Buffers with differential pairs are of the simplest structures we can do and they will be able to help measurements. In addition, we will be able to evaluate the speed / load obtained for each structure in different technologies, at different temperatures.

3.4.4. Building Blocks to be Evaluated

3.4.4.1 CML building blocks

The high drive current measured for III-V nanowire MOSFETs make them good candidates for CML circuitry. To evaluate their performance in HPC and Edge AI applications, basic building blocks including inverters and latches will be designed, fabricated and evaluated at various temperatures. The circuits will consist of vertical InGaAs nanowire MOSFETs that will be combined with integrated resistors for the CML building blocks.

3.4.4.2 Ring Oscillator for High Performance Computing

This building block will be designed to evaluate the digital speed of the technology at cryogenic temperature, in comparison to room temperature performances. The assumption that silicon CMOS transistors perform better at low temperature may be invalid below 40K since physical effects may deteriorate device performance.

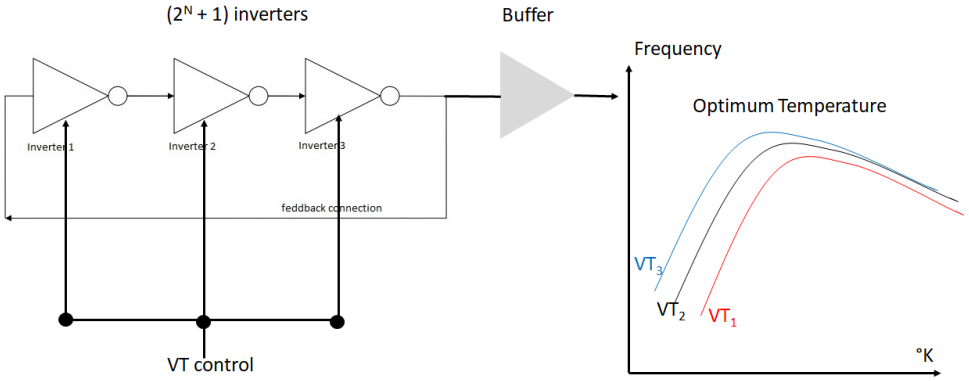

Figure 2: Ring Oscillator with V_T control schematic and forecasted frequency performance.

The Ring oscillator will be designed in 28nm FDSOI process. By taking advantage of the back-gate bias, the transistors threshold voltage (V_T) will be controlled, in order to find the best speed compromise versus the temperature. This will define the minimum transit time in an inverter, the F_T value, and therefore the predicted digital speed improvement as compared to room temperature.

3.4.4.3 DFF and Scrambler

DFF building block will be designed to define set-up and hold time, the simplest structure to evaluate such times is the divider by 2, where the smallest clock period is directly in line with the sum of set-up and hold times. In addition, and depending on the man-power means, the scrambler structure could be put in place, this one will give additional information on rise and fall times through the eye diagram.

FDSOI: In the same approach as described for the Ring oscillator design, an FDSOI DFF in CMOS logic with V_T control will be designed and assembled in a divider by 2. Depending on man power means, it is envisaged to study a scrambler structure.

III-V Nanowire MOSFETs: Building on the studies on the CML inverters and latches, more complex structures can be designed and fabricated. With the goal to evaluate the potential performance in the temperature range of 40-70K, we will design more complex circuits using III-V nanowire MOSFETs. Depending on available man months, the circuit may be implemented.

3.4.4.4 Buffer

The Buffer structures can be either based on CMOS logic, or CML logic, they will be designed isolating internal structures, and also, defining which impedance can be loaded at high frequency.

FDSOI: A buffer structure, will be designed in order to isolate internal structures, and to allow testing. This Buffer will be done in a CMOS logic approach, with V_T control.

4 Wireless Wideband Communication and Sensing at Room Temperature

4.1 Introduction

4.1.1. Wireless Wideband Communications at Room Temperature

Wireless wideband communications are mainly driven by 5G, beyond 5G and 6G telecommunication evolutions. The first analysis done in this deliverable was to define which future 6G bands will be explored by the European 5GPPP organization, and how these bands are treated worldwide. 6G evolution targets mainly two frequency band domains: the well-known mmW to THz, or more accurately 100-300 GHz range, where wide band is easy to obtain, but, where link budget is very hard to obtain and the sub-20 GHz bands where

there is room for new bands to be used to obtain high data rate communications. For high data rate communications, signal processing is more challenging than the link budget, as km distance ranges can be targeted. The frequencies explored for sub-20GHz bands as defined in the *Beyond 5G Report* (https://www.rrt.lt/wp-content/uploads/2019/05/Beyond-5G-final-.final-1-1.pdf) are shown in figure 3.

- to consider additional spectrum allocations to the mobile service on a primary basis when required and identification of additional spectrum within the frequency bands 3.8-4.2 GHz, 6425-8500 MHz and 14.3-15.35 GHz for International Mobile Telecommunications (IMT), to secure future development of terrestrial mobile broadband applications

Contribution	Proposal for new agenda item for WRC-23 to study additional spectrum for IMT
035 (ETNO)	3800-4200 MHz, 6425-8500 MHz, 14.3-15.35 GHz
036 (GSMA)	3300-3400 MHz, 3800-4200 MHz, 7125-8500 MHz, 10.7-11.7 GHz, 14.5-15.35 GHz
062 (Ericsson, Huawei)	6425-7125 MHz
INFO01 (RUS)	Above 6525 MHz, in particular 6525-7100 MHz

Figure 3: Explored bands under 20GHz for IMT to secure Beyond 5G to 6G

This opens an opportunity to explore these bands for 5G to 6G communications, in addition a circuit covering this request would be in line with SPIN based Quantum computing Qubit manipulation signal which should cover frequency band up to 20GHz, following the first discussion we had in WP3, and the D3.1 deliverable. This means that, there is a very nice opportunity to develop signal generation for this sub-20GHz band.

Coming back to the mmW to THz communications, the first approach was to analyse the spectrum, to define which bands can be used, figure 4 presents the future 6G mmW to THz Bands and the atmospheric absorption coefficient versus frequency.

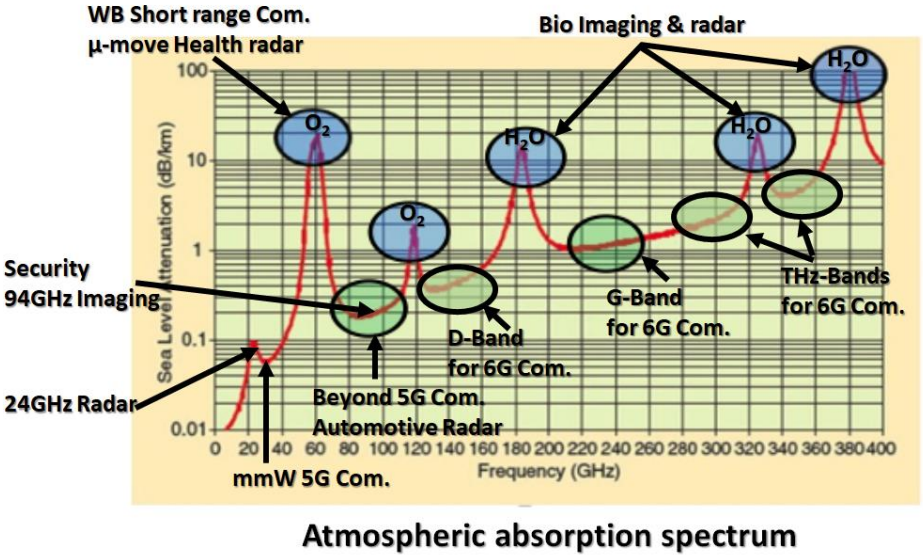

Figure 4: mmW Bands for applications and atmospheric absorption spectrum

As presented in the figure above, the first mmW to THz 6G band is the D-Band between 110 GHz and 170 GHz, even if it is very difficult to exploit a 40% bandwidth over carrier frequency, this band offers 60 GHz bandwidth

which means data-rates in the range of 100 Gbs to 400 Gbs depending on the modulation complexity. G-Band and THz-Band offer more than this, but at higher frequency than 220 GHz and 280 GHz. Technology proposed in cryogenic technology platform have F_{max} between 300 GHz and 600 GHz, which allow to cover the whole D-Band, even if some tries can be done at higher frequency.

For this frequency band domain, taking into account the technology properties, and the telecommunication interest, the consortium has focused its interest on the D-Band.

4.1.2. Sensing at Room Temperature

Looking at the atmospheric absorption spectrum figure, we can notice the different peaks of absorption, at 60GHz, 120GHz, 180GHz, 325GHz, and 380GHz. The two first peaks are due to oxygen molecule energy absorption, while the last three ones are due to the H_2O molecule. These properties are very interesting for sensors, at 60GHz a lot of work has been done around the wideband short-range communication, and recently people have begun to study health radar applications, measuring body micro-move (heart and breathing) in mm range. Bands over 180GHz are very interesting to discriminate humid tissues from dry ones, and the higher the frequency, the better the accuracy.

Huge work has yet been done by the consortium in the 60 GHz band, and possibly, circuit will be evaluated in this band. 180 GHz is more relevant, depending on the performances obtained for D-Band communications, circuit could be evaluated for this frequency.

4.2 Building Blocks Description

Building blocks proposed in this chapter will be studied in Task 4.1, part of them will be also studied in WP3 for Qubit manipulation and readout functions.

4.2.1. The Multi Frequency Generation Building Block

The multi Frequency generation building block will target sub-20GHz communication and then the SPIN Qubit manipulation applications implemented in FDSOI process. The mmW to THz D-Band could also be explored with the existing circuit.

4.2.2. Technologies to be Explored

As described for previous contributions, FDSOI process seems suitable in order to potentially exploit the back-gate Threshold voltage modulation capability. Moreover, FDSOI technology offers the capability to co-integrate analog and digital functions with a good overall performance. Even if it appears that a quantum system might be partitioned through various temperature stages, the boundaries are not clearly fixed. Using a same technology platform for analog and digital parts, or cold and room temperature segments, ensures flexibility.

However, if time and resources allow it, the consortium keeps the opportunity to characterize at low temperature some blocks that where already done with other technologies, like 45RFSOI. This optional task is sustained by the interest of comparing some specific designs on different technologies when temperature shifts down. A 45RFSOI D-Band Multi-frequency source could be evaluated following this methodology.

4.2.2.1 Analog Architecture for Wideband Communication and Sensing at Room Temperature in Relation to Quantum Carrier Driving

At a first view, a scalable approach for Qubits reading/writing will require electronics that is able to manage a wide frequency plan, covering the spectrum from few hundreds of MHz to about ten GHz and more, with various waveforms and dynamics. Of course, it depends on the number, and the technology of Qubits. Even

if it also depends on the reading/writing system strategy, the state of the art suggests that many challenges should be met in order to read or write an ensemble of Qubits correctly. These challenges can be aggregated into a set of circuit parameters: Signal to Noise Ratio, Spurious Free Dynamic Range, Phase tracking accuracy, Pulse shape accuracy, Voltage sensitivity, Noise Figure and Oscillator Phase Noise.

As mentioned before, such a system would be split into several parts, distributed along various temperature stages. Some very critical blocks will be close to the Qubits, whereas some consuming blocks should stay at higher temperature. According to the internationally shared knowledge, it is still open which temperatures to target for this division. Two main parameters will probably drive the partitioning: the power consumption/dissipation, and the loss through the interconnects. Beside the research on technology innovations (superconductor's integration, low V_T CMOS transistors, III/V technologies…), some experts who explore electronic innovations are turning toward multiplexing architectures.

These general considerations (that where already introduced and illustrated in the technical annex of the project), lead to think that should be pivotal to design a very efficient multiple frequency synthesis, one of the key blocks of such a system.

4.2.2.2 Block to Explore to Achieve the Demonstration of Interest

Based on the experience of the consortium in the field of mmW radars and 5G-6G digital communications, we will develop a multiple frequency synthesis from few 100's MHz to 10-15GHz, that is inspired from the knowledge of TORP architecture (Oscillations Trains Periodically Repeated). Figure 5 explains succinctly the principle of operation.

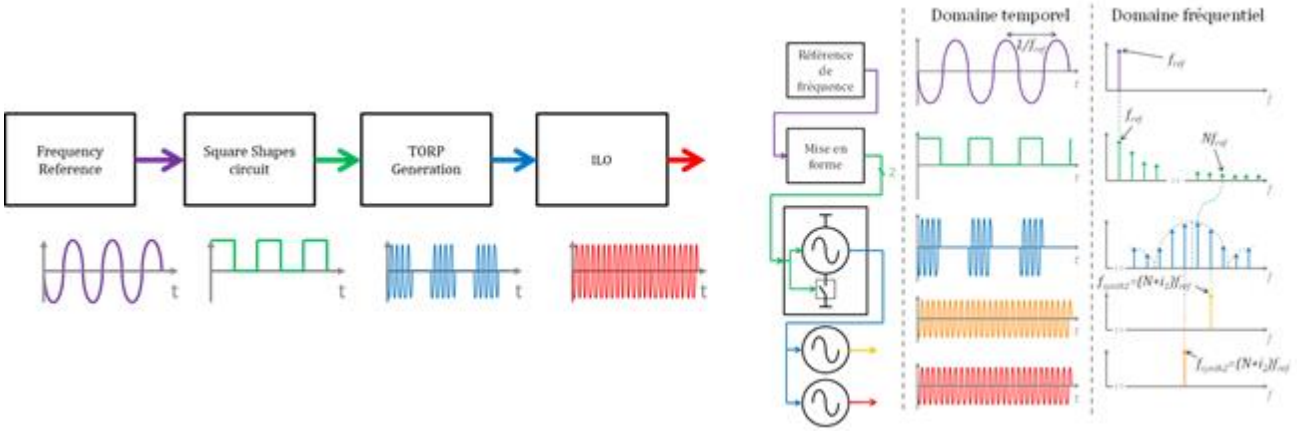

Figure 5: TORP architecture (Oscillations Trains Periodically Repeated) principle

When a low frequency reference is used to periodically mute an oscillator, it generates a wide spectrum of Dirac rays where the overall envelope is modulated by a cardinal sinus function. Not only does it produce a multiple frequency source, but also it copies the reference phase noise at each frequency, applying only the frequency shift additional contribution. Therefore, this reference can drive a set of ILO's (Injection Locked Oscillator) to obtain a set of higher frequency low phase noise continuous waves. With this technique, the multiplication factor can reach about 30, where classical frequency generators are limited around to 5.

This block (Frequency synthesis and a few ILO's) will be designed at lower frequency than usually. We will evaluate the performance and the footprint at such frequency range, and we hope to investigate its behaviour at room temperature as well as at low temperature. Especially, if ILO's can operate at cryogenic temperatures with a very low power budget, it would open the door to a smart multiplexing approach, where ILO's could be attached to individual Qubit drivers.

This 28nm FDSOI Building block will be evaluated at Room temperature in the 5G context, at 40K-70K evaluating the potentiality to serve as frequency synthesis for cryogenic temperature, and to evaluate the temperature impact on the phase noise, and frequency stability, and then it could be evaluated at sub-4K for Qubit application, if results at 40-70K are good enough.

4.2.3. UWB Sub-15-GHz LNA

Ultrawideband (UWB) systems allow to transmit data over a wide spectrum of frequency bands with very low power and high data rates. UWB technology may be used for Wireless WideBand communication and sensing systems but also for imaging systems, vehicular and ground-penetrating radars. To improve sensitivity and reduce consumption of current UWB systems, we propose to design in 28-nm FD-SOI technology an UWB sub-15-GHz LNA (in line with Quantum Computing) and characterize it at 40K-70K within the new sub-15-GHz frequency bands proposed from IMT for beyond 5G (https://www.rrt.lt/wp-content/uploads/2019/05/Beyond-5G-final-.final-1-1.pdf).

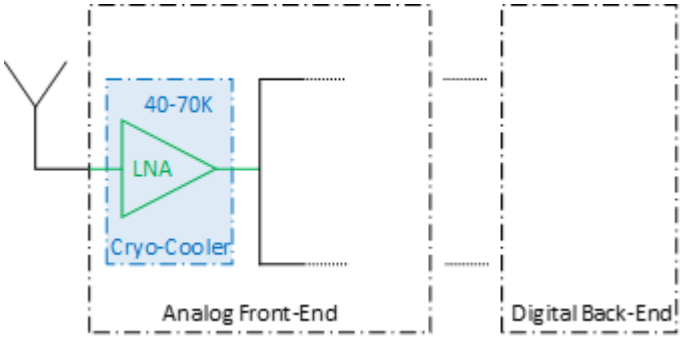

Fig. 6. Receiver of UWB sub-15GHz system

The designed UWB LNA requires wideband input matching to a 50-Ohm antenna, filtering of out-of-band interferers, flat gain over the entire bandwidth, good linearity, noise figure (NF) minimization and low power consumption. This designed block can address the section 2.2 and operate in wireless Space 40-70K communication and sensing systems.

This 28nm FDSOI Building block will be evaluated at Room temperature in the 5G context, at 40K-70K evaluating the potentiality to serve the space applications, and to evaluate the temperature impact on the Noise figure, and then, it could be evaluated at sub-4K for Qubit application, if results at 40-70K are good enough.

However, if time and resource allow it, the consortium keeps the opportunity to characterize at low temperature some blocks that where already done with other technologies, like 45RFSOI. This optional task is sustained by the interest of comparing some specific designs on different technologies when temperature shifts down. A 45RFSOI 5G LNA + Switch could be evaluated following this methodology.

4.2.4. Building Blocks for Integration of LNAs and RF Switches

D-Band 110GHz LNA and switch blocks in vertical nanowire transistor technology (f_T/f_{max}=340/390 GHz) have been studied for use as a suitable demonstrator circuits for beyond 5G at 110 GHz. The LNA design is focusing on a differential 2 stages topology meeting expected 5G requirements, regarding bandwidth, Noise Figure (NF), linearity and compression. Insertion loss of transformers reflects the performance of the BEOL of the transistor technology.

Starting point for the switch design is a SPDT topology, as proposed by Fabian Thomé et.al. A suitable compromise between insertion loss and isolation for Beyond 5G D-band allocation is obtained. Benchmark performance comparison shows to be on par with more dedicated technologies.

Key performance metrics like noise figure for an Integrated LNA and Switch solution meets expected 5G requirements.

Different switch topologies with and without transmission lines have been studied and compared for the vertical nanowire transistor technology.

5 Summary

In Work Package 4 we will explore four main FET structures: III-V mHEMT and MOSHEMT from IAF; III-V nanowires from ULUND; Tunnel FET from ULUND; and 28nmFDSOI from LETI, at two temperature ranges: 40-70K and room temperature, for 6 applicative usages: Satellite sensing; satellite communications; High performance computing; edge computing; terrestrial communication, and room temperature sensing. The list of designed building blocks and their applicative domains and processes are given below. In addition, the consortium, depending on the man-power and time availability, forecasts to extend the list to the DFF based scrambler structures, and to evaluate others processes with existing IPs they have yet designed. Part of these blocks will serve also Quantum computing application, and will be developed in close collaboration with WP3.

Table 1: WP4 Building Blocks study forecast

Building Blocks	Satellite Sensing 40 - 70K	Satellite Communication 40-70K	HPC 40 - 70K	Edge Computing IoT @ RT	Communication @ RT	Sensing @ RT
In SEQUENCE Design						
E Band Comm LNA		mHEMT - MOSHEMT			mHEMT - MOSHEMT	
89GHz Sense LNA	mHEMT - MOSHEMT					mHEMT - MOSHEMT
E Band RF swiches SPDT		mHEMT - MOSHEMT			mHEMT - MOSHEMT	
E Band Quadrature LO		III-V nano-wire FET			III-V nano-wire FET	
CMOS Ring Osc. + VT control			28nm FDSOI	28nm FDSOI		
CMOS DFF			28nm FDSOI	28nm FDSOI		
CMOS Div By 2 based on DFF			28nm FDSOI	28nm FDSOI		
CMOS Buffer			28nm FDSOI	28nm FDSOI		
Low voltage differential amplifier			Tunel FET	Tunel FET		
CML Inverter			III-V nano-wire FET	III-V nano-wire FET		
CML DFF Design			III-V nano-wire FET	III-V nano-wire FET		
CML Div By 2 based on DFF Design			III-V nano-wire FET	III-V nano-wire FET		
Differential Buffer Design			III-V nano-wire FET	III-V nano-wire FET		
Sub-20GHz Multi-freq. Gene.		28nm FDSOI			28nm FDSOI	
Sub-15GHz Wide Band LNA		28nm FDSOI			28nm FDSOI	
D-Band LNA		III-V nano-wire FET			III-V nano-wire FET	
D-Band Switch		III-V nano-wire FET			III-V nano-wire FET	
Potential extended design						
DFF Based Scrambler structures			III-V nano-wire FET / FDSOI	III-V nano-wire FET / FDSOI		
Potential Test of existing Blocks						
D-Band Multi-Freq Gene.		RFSOI 45nm			RFSOI 45nm	
5G LNA + Switch		RFSOI 45nm			RFSOI 45nm	
60GHz Blocks to be defined	65nm CMOS / 28 FDSOI ?					65nm CMOS / 28 FDSOI ?

With this experimentation feedback, the consortium targets finding other applicative fields for the Cryogenic Technology Platform, and also, benchmarking this platform to other potential competitive processes evaluated in this work package.