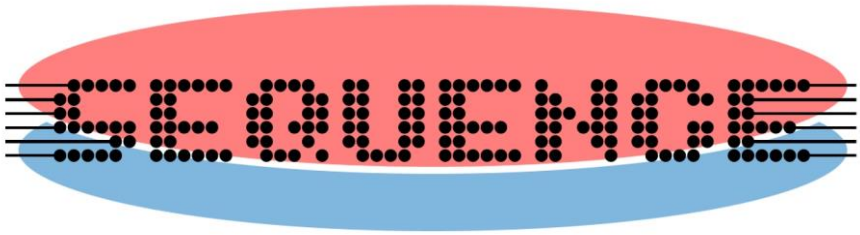
Deliverable – D2.2

Report on first version of device compact models for LF and RF circuit simulation



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1 Introduction

The SEQUENCE project offers a unique opportunity to perform characterization and modelling of various Si and III-V devices and use them in electronics for quantum computing and communication applications. The modelling effort within SEQUENCE covers the modelling of a) new effects appearing in devices operating at low temperature in order to better understand the better understand the physics that govern these phenomena, b) the compact modelling of such phenomena so that they can be embedded in compact models available for the design and c) simplified models that can help the circuit designers in better sizing their circuit to optimize their performance at low temperature. A good example is the modelling of the saturation of the subthreshold swing that is observed at low temperature. It was first characterized experimentally [1] and modelled using a physics based model [1] [2] and finally a physics-based empirical model that is simple enough to include in a compact model [3]. Now a compact model would be useless without clear parameter extraction procedures.

In this perspective, the objectives of WP2 is to perform an electrical characterization, develop analytical compact device models and the associated parameter extraction that are valid at very low temperature and usable for circuit design. This deliverable reports on first version of device compact models available for circuit simulation.

Section 2 starts with a short introduction to the EKV charge-based model. It shows how it can be used for early characterization but can also be a very useful tool to guide circuit designers selecting the appropriate size and bias point for their analogue circuits to optimize performance and in particular power consumption. It also presents the tool that was developed for doing an efficient and automatic parameter extraction of the EKV model parameters which are valid at low temperature.

Section 3 presents Poisson-Schrödinger simulations and an analytical charge model for a back biased FDSOI structure operated at deep cryogenic temperatures. INPG and LETI have established a set of analytical equations based on a single subband scheme within an Airy's function approach, providing a good description of the surface potential, the inversion charge and the capacitance characteristics of FDSOI structures operated at very low temperature and for various back bias and silicon thickness. This analytical charge model is a first step towards a cryogenic compact model for FDSOI MOSFET with back biasing action, which will be transferred to UTSOI LETI platform in the near future.

Section 4 presents a highly scalable in terms of transistor geometry (gate-width, finger number) and temperature dependent distributed small-signal HEMT model. The model has been validated with IAF's 50 nm mHEMT technology with on-wafer S-parameter measurements performed at room and at cryogenic temperatures. It is shown that the model is able to correctly reproduce the measurements up to at least 150 GHz and at arbitrary temperatures between 10 K and 300 K. This is achieved by precise modeling of the temperature dependency of the various equivalent circuit elements building the model.

Section 5 presents a large-signal compact model for III-V nanowire MOSFETs and TFETs based on the virtual source model augmented with physical parameters and geometrical scaling. It is shown that the model fits the IV characteristics very well.

Conclusions and future perspectives are given in Section 6.

2 EKV charge-based DC model for bulk and FDSOI devices

This Section introduces the EKV compact model that is used to characterize the MOSFET transistor operation at room and at cryogenic temperatures in terms of the inversion level measured by the inversion coefficient. The model is formulated in a normalized way and the normalization parameters basically allow to capture a given technology and device by four parameters (five for FDSOI). The model can also express important figures-of-merit (FoMs) in terms of these parameters and the inversion coefficient which becomes the main design parameters. In this way the model can help the designer to explore the design space and better optimize their circuits by choosing the appropriate device size and bias point.

In the SEQUENCE project, it is proposed to investigate whether this same model is still valid at cryogenic temperatures. If this is the case it can then be used by designers to design analogue and RF circuits needed to interface the qubits. This is particularly useful, because full compact models that are available in PDKs are not yet accurate at cryogenic temperatures. It will take some time to have these industry standard compact models be updated to also work at cryogenic temperatures. In the meantime, the designer can therefore use the simple EKV model to start his design.

This Section gives a short introduction to the EKV charge-based compact model and the concept of inversion coefficient. It then presents the most important FoM and how they depend on the inversion coefficient. A parameter extraction tool has been developed to automatically extract the main EKV parameters from data measured at room and at cryogenic temperatures.

2.1 The EKV Charge Based Model

The EKV charge-based MOSFET model has initially been developed in the 90s for low-power analogue circuit design. It better accounted for the regions of moderate and weak inversion (WI) in a continuous way avoiding the discontinuities that other early compact models such as BSIM3 faced in the region of moderate inversion (MI) [4] [5]. This work led to the initial version 2.6 of the EKV compact model which has only a few parameters and is available in many circuit simulators. The later model showed its limit and a new version 3 full-fetched charge-based compact model was then developed to better cope with more advanced CMOS technologies, but keeping the original target of low-power analogue IC design [6]. As technology was scaling and performance were increasing, the EKV model was used for the design of RF circuits biased in MI and WI [7]. The core of the EKV model was then used in the industry-standard BSIM 6 compact model which became later the BSIM-bulk model [8]. The EKV model was also used for the design of analogue front-end operating at low-temperature [9]

In the recent years, a simplified version of the charge-based EKV, named sEKV, that only requires 4 parameters was proposed [10] [11]. The purpose of this model is to help designers explore the design space and better optimize their circuit for low-power operation. The model can also be used to quickly assess and compare various technology from an analogue and RF circuit design perspective [12] [13] [14].

The down-scaling of CMOS processes and the reduction of the supply voltage has progressively pushed the operating point from the traditional strong inversion (SI) region towards moderate (MI) and even weak inversion (WI), where the simple quadratic model is obviously no more valid [14] [15]. This trend is illustrated in Figure 1, which shows the normalized drain current in saturation (actually corresponding to the inversion coefficient defined below) versus the gate voltage assuming a 0.5 V supply voltage. The red curve shows the result for a CMOS-bulk process with a threshold voltage of 200 mV, whereas the blue curves shows the I_D-V_G for a FDSOI process for threshold voltages of 200 mV and 150 mV.

We clearly see that the transistor can no more reach strong inversion even when applying the maximum gate voltage. SI will therefore disappear with voltage scaling highlighting the motivations for having a simple model that covers WI and MI in a continuous way.

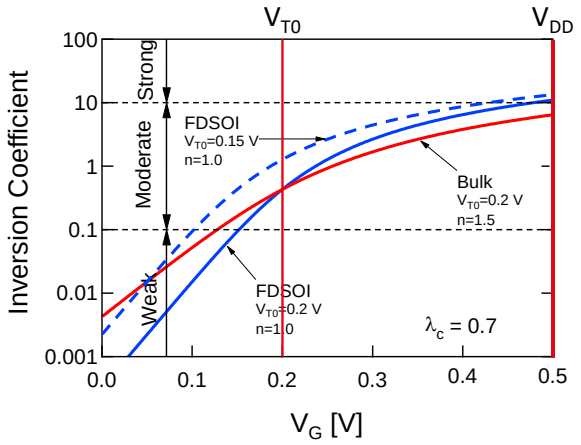


Figure 1: Strong inversion will disappear at low supply voltage.

This recent trend has led to an increased interest in the concept of inversion coefficient as the main design parameter replacing the overdrive voltage even for advanced technologies [16] [17]. The inversion coefficient IC is a measure of the inversion level in the channel of a single MOSFET and is defined as [5]

$$IC = \frac{I_D|_{\text{saturation}}}{I_{spec}} \tag{1}$$

where the normalizing factor I_{spec} is called the specific current, and is defined as [5]

$$I_{spec} \triangleq I_{spec\blacksquare} \cdot \frac{W}{L} \text{ with } I_{spec\blacksquare} \triangleq 2n \cdot \mu_0 \cdot C_{ox} \cdot U_T^2 \tag{2}$$

Where W and L are the width and length of the transistor, n is the slope factor, μ_0 is the low field mobility in the channel region, C_{ox} the oxide capacitance per unit area and $U_T \triangleq kT/q$ is the thermodynamic voltage. In a given technology, the specific currents per square $I_{spec\blacksquare}$, one for each transistor type (n- and p-channel), are the most fundamental parameters for the designer. Using IC, the different regions of operation of a MOSFET can be classified as illustrated in Figure 2 and defined below

$$\begin{array}{cc} IC \leq 0.1 & \text{weak inversion (WI)} \\ 0.1 < IC \leq 10 & \text{moderate inversion (MI)} \\ 10 < IC & \text{strong inversion (SI)} \end{array} \tag{3}$$

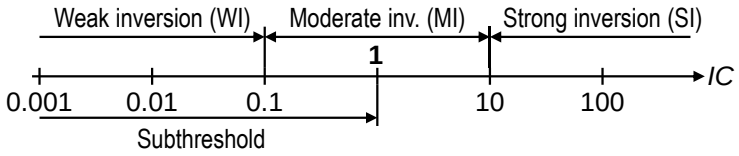


Figure 2: The different regions of operation in terms of inversion coefficient.

The drain current in saturation normalized to the specific current, which according to (2) corresponds to the inversion coefficient IC defined above, is given by

$$IC = \frac{I_D|_{\text{saturation}}}{I_{spec}} = \frac{4(q_s^2 + q_s)}{2 + \lambda_c + \sqrt{\lambda_c^2(2q_s + 1)^2 + 4(1 + \lambda_c)}}, \quad (4)$$

where q_s is the normalized inversion charge $q_s \triangleq Q_i(x = 0)/Q_{spec}$ taken at the source with $Q_{spec} = -2nC_{ox}U_T$ [5]. Parameter λ_c is accounting for velocity saturation (VS) according to

$$\lambda_c = \frac{L_{sat}}{L} \quad (5)$$

and scales inversely proportional to the transistor length L. Parameter λ_c actually corresponds to the fraction of the channel in which the carrier drift velocity reaches the saturated velocity v_{sat} over a portion of the channel length $L_{sat} = 2\mu_0 U_T/v_{sat} = 2U_T/E_c$. The normalized source charge q_s is related to the terminal voltages by [5]

$$v_p - v_s \triangleq \frac{V_P - V_S}{U_T} = \ln(q_s) + 2q_s, \quad (6)$$

where $v_p - v_s$ is the saturation voltage $V_P - V_S$ normalized to U_T, $V_P \cong (V_G - V_{T0})/n$ is the pinch-off voltage and V_S is the source-to-bulk voltage. Note that in the EKV model, all the terminal voltages are referred to the local substrate instead of the source terminal, in order to preserve the symmetry of the device in the model [5].

The normalized saturation voltage can be expressed in terms of the inversion coefficient IC by solving (4) for q_s leading to

$$q_s = \frac{1}{2} \cdot \left(\sqrt{4IC + (1 + \lambda_c \cdot IC)^2} - 1\right) \quad (7)$$

and using (7) in (6). Unfortunately, (6) cannot be inverted to express IC in terms of $V_P - V_S$ and hence of the terminal voltages.

The most important small-signal parameter is without doubt the gate transconductance G_m. Since in the EKV model the voltages are all referred to the bulk, we can define two other transconductances: the source transconductance $G_{ms} \triangleq -\partial I_D/\partial V_S$ and the drain transconductance $G_{md} \triangleq \partial I_D/\partial V_S$ [5]. Note that G_{md} should not be confused with the output conductance G_{ds}. In saturation $G_{md} = 0$ and $G_{ms} = n \cdot G_m$. The normalized source transconductance in saturation g_{ms} can be expressed in terms of IC as

$$g_{ms} \triangleq \frac{G_{ms}}{G_{spec}} = \frac{\sqrt{(\lambda_c \cdot IC + 1)^2 + 4IC} - 1}{\lambda_c \cdot (\lambda_c \cdot IC + 1) + 2} \quad (8)$$

where $G_{spec} \triangleq I_{spec}/U_T = 2n \cdot \mu_0 \cdot C_{ox} \cdot U_T$. Note that for short-channel devices in SI, the I_D-V_G transfer characteristic becomes a linear function of the gate voltage and hence the gate transconductance becomes independent of the drain current and of the gate length L. It then only depends on W and v_{sat} according to

$$g_{ms} \cong \frac{1}{\lambda_c} \text{ for } IC \gg 1 \text{ or } G_{ms} \cong W \cdot C_{ox} \cdot v_{sat}. \quad (9)$$

The inverse of the VS parameter λ_c is therefore a key parameter since it gives the maximum normalized transconductance that can be achieved for a short-channel device in a given technology.

This simplified charge-based model only requires four parameters to fit the I_D-V_G transfer characteristic: the slope factor n, the specific current per square $I_{spec\blacksquare}$, the threshold voltage V_{T0} and the velocity saturation parameter λ_c or L_{sat}. Since the normalized characteristics remain almost identical for various devices and processes, these 4 parameters basically capture the most important features of the technology and device. They can therefore be used to assess and compare various devices

and technologies. The methodology and the platform that was developed for extracting these parameters automatically from measurements is explained in Section 2.3. This Section also gives new results from measurements at RT of various devices from a 22 nm FDSOI technology and 17 nm FinFET technology. The same devices will be measured at cryogenic temperature and the tool will be used to extract the same EKV parameters for each temperature.

Although initially developed for bulk MOSFET, this model has also been successfully used for FDSOI and FinFET devices. Examples of I-V characteristics are shown in Section 2.3 where the excellent fits are obtained. An additional parameter is required to also account for the back-gate voltage, increasing the number of parameters to five.

2.2 Basic Figures-of-Merit (FoM)

The transconductance efficiency or current efficiency G_m/I_D , is one of the most important figure-of-merit (FoM) for low-power analogue circuit design. It is a measure of how much transconductance is produced for a given bias current and is a function of C . In normalized form, the transconductance efficiency is defined as the actual transconductance obtained at a given IC with respect to the maximum transconductance $G_m = I_D/(nU_T)$ reached in WI

$$\frac{G_{ms} \cdot U_T}{I_D} = \frac{G_m \cdot n \cdot U_T}{I_D} = \frac{g_{ms}}{IC} = \frac{\sqrt{(\lambda_c \cdot IC + 1)^2 + 4IC} - 1}{IC \cdot (\lambda_c \cdot (\lambda_c \cdot IC + 1) + 2)} \tag{10}$$

Expression (10), which is continuous from WI to SI and includes the effect of velocity saturation (VS) through the λ_c parameter, is plotted in Figure 3. It is remarkable that (10) actually only requires a single parameter λ_c in addition to the slope factor n used for the y-axis normalization and the specific current I_{spec} used for the x-axis normalization. It is completely "voltage agnostic" since the threshold voltage does not appear in this expression. The figure shows that $G_m \cdot nU_T/I_D$ is maximum in WI and decreases as $1/\sqrt{IC}$ in SI for long-channel devices in which VS is absent (dashed blue curve). For short-channel devices subject to VS, the drain current becomes a linear function of the gate voltage, independent of the transistor length. Hence, the transconductance becomes independent of the current and of the length. Since G_m becomes independent of I_D or of IC , the $G_m \cdot nU_T/I_D$ curve scales like $1/(\lambda_c IC)$ in SI instead of $1/\sqrt{IC}$ when VS is absent. In essence, the effect of VS is to degrade the transconductance efficiency in SI, meaning that more current is required to reach the same transconductance obtained without VS. Nevertheless, irrespective of the channel length, $G_m \cdot nU_T/I_D$ remains invariant in WI, since short-channel effects (SCE), including VS, have the same effect on G_m than on I_D simply because G_m is proportional to I_D in WI.

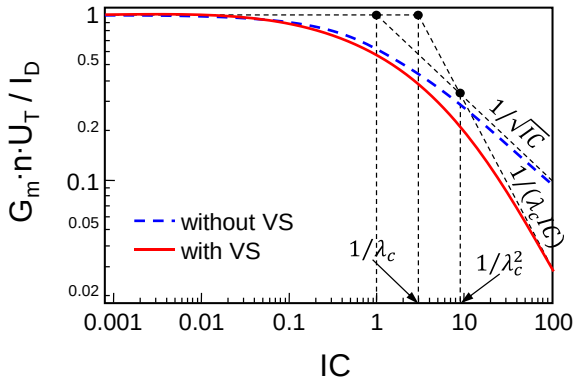
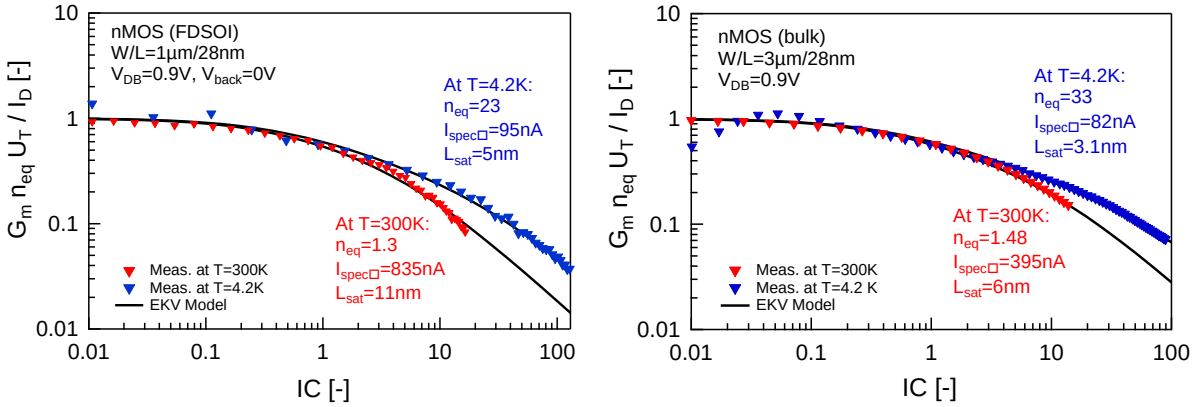


Figure 3: The current efficiency g_{ms}/IC versus IC showing the effect of velocity saturation VS) occurring for short-channel devices.



a) 28-nm bulk CMOS process. *b) 28-nm FDSOI process.*

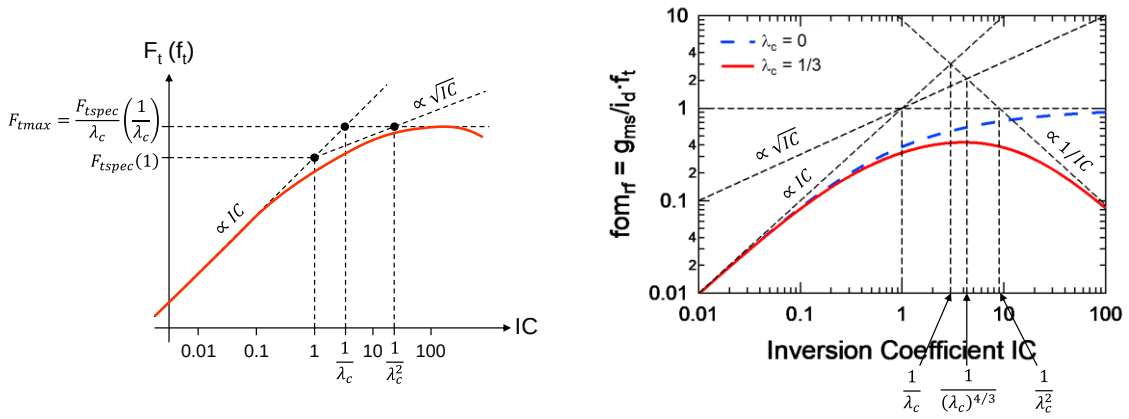
Figure 4: Normalized G_m/I_D vs. IC characteristics for 28-nm processes measured at RT and at LH.

The normalized G_m/I_D of a bulk and FDSOI 28-nm processes have been measured at RT and at liquid Helium (LH) resulting in the plots shown in Figure 4. We see that thanks to the normalization the characteristics at RT and LH are very close. The difference arises from the value of the velocity parameter λ_c which is different at RT and LH because λ_c is inversely proportional to v_{sat} which is higher at LH temperature and hence moves the intersection point to higher values of IC.

Another FoM useful for assessing the RF capability of a given device and process is the transit frequency F_t given by

$$F_t = \frac{1}{2\pi} \cdot \frac{G_m}{C_G} \tag{11}$$

where $C_G = C_{Gi} + C_{Ge}$ is the total gate capacitance comprising of the intrinsic capacitance C_{Gi}, which is linked to the mobile charges in the channel, and the extrinsic capacitance $C_{Ge} = C_{GeW} \cdot W$, including the overlap and fringing field capacitances, which both scale with the transistor width W. For short-channel devices, the total capacitance is dominated by the extrinsic capacitance C_{Ge} which is almost bias independent. The bias dependence of F_t therefore mostly follows that of G_m as illustrated in Figure 3. In WI, $g_m \propto IC$ and hence F_t is also proportional to IC.



a) The transit frequency F_t vs. IC showing the definition of F_{tspec}. The variables in parenthesis correspond to the normalized transit frequency.

b) Normalized figure-of-merit fom_{rf} (on a log scale) vs. IC, along with the WI and SI asymptotes.

Figure 5: RF FoM versus IC.

Similarly to G_m/I_D, F_t can be normalized as shown in Figure 5 a) to F_{tspec} defined as the value of F_t on the WI asymptote corresponding to $IC = 1$ [12]. In this way, the normalized transit frequency $f_t \triangleq F_t/F_{tspec}$ turns out to be equal to g_{ms} which is given by (8). Note that F_{tspec} scales roughly as $1/L$ [12]

$$F_{tspec} = \frac{I_{spec}}{2\pi n U_T C_{GeW} L}. \tag{12}$$

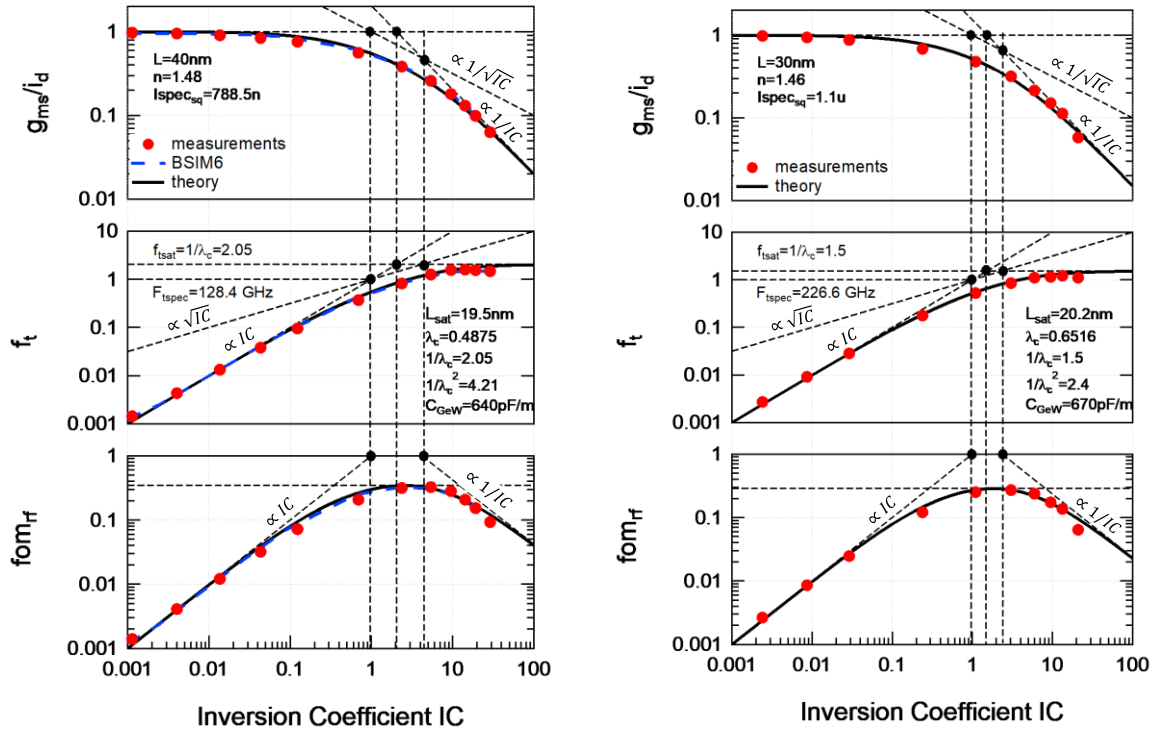
As illustrated in Figure 5 a), in SI and under VS (i.e. for $1/\lambda_c^2 < IC$), F_t (or f_t in normalized form) saturates to F_{tspec}/λ_c (or simply $1/\lambda_c$ in normalized form). Note that once the VS parameter is extracted from the G_m/I_D as described in [10], it is therefore easy to assess the peak F_{tspec} for a given technology from F_{tspec}. It is also interesting to point out that the denormalized value of the saturation value of F_t is given by [12]

$$F_{tpeak} = \frac{F_{tspec}}{\lambda_c} = \frac{WC_{ox}v_{sat}}{2\pi C_G} \cong v_{sat} \cdot \frac{C_{ox}}{2\pi C_{GeW}}, \tag{13}$$

which shows that surprisingly F_{tpeak} does not scale as $1/L$ anymore [12]. This means that the only way to increase F_{tpeak} is to increase C_{ox} but without increasing C_{GeW} [12]. This result may be key when operating the device at cryogenic temperatures. The only parameter that depends on temperature is the saturated drift velocity v_{sat} which should increase slightly at low-temperature.

There exists a fundamental trade-off between the G_m/I_D and F_t FoMs. Indeed, aiming for low-power operation by targeting a high G_m/I_D at small values of IC invariably means compromising in speed (bandwidth). Combining the two FoMs that have their maxima on the opposite ends of the IC axis, the $G_m/I_D \cdot F_t$ FoM serves as design guide to locate the optimum IC [18] [19] [20]. As shown in Figure 5 b), this FoM shows a maximum that lies right in the middle of the MI region, which is identified as a good trade-off between high F_t and low-power. The 3 FoMs presented above are plotted versus IC in Figure 6 for a 40- and a 30-nm RF device from a 40- and 28-nm bulk CMOS process, respectively [12] [11]. Despite its simplicity and reduced number of parameters, the analytical models fit very well the experimental data over almost 5 decades of IC (or current).

To our knowledge both FoMs F_t and $G_m/I_D \cdot F_t$ have not been reported at cryogenic temperature yet. We will conduct these measurements to check whether the models remain valid at cryogenic temperatures.



a) 40 nm bulk CMOS process. *b) 28 nm bulk CMOS process.*

Figure 6: The 3 key FoM, $G_m \cdot nU_T/I_D$, f_t and $G_m \cdot f_t/I_D$ versus IC.

A key building block in the CMOS interface to the qubits is the low-noise amplifier (LNA). At RF the noise is dominated by the white noise of the input device which may be thermal or flicker noise depending on the regime in which the input transistors are biased (thermal noise if biased in SI and shot noise if biased in WI). Operating the LNA at LT may therefore allow to reach very low noise figures at reduced power consumption compared to RT. The noise performance of an LNA is characterized by another FoM called the noise excess factor γ defined as

$$\gamma \triangleq G_m \cdot R_n, \tag{14}$$

where R_n is the input-referred thermal noise resistance. For long-channel devices γ is equal to $\gamma = 2/3 \cdot n \cong 1$ in SI and $\gamma = n/2$ in WI. As shown in Figure 7, this noise excess factor significantly degrades (increases) in SI for short-channel devices from various technologies. This increase of γ with respect to IC can be modelled empirically by

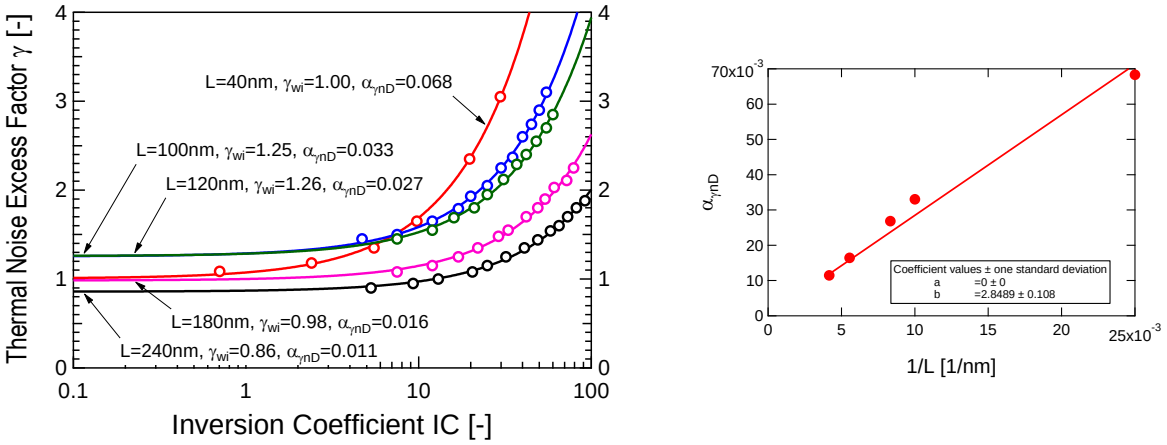
$$\gamma \cong \gamma_{wi} + \alpha_{\gamma_{nD}} \cdot IC, \tag{15}$$

where $\alpha_{\gamma_{nD}}$ is an empirical factor that scales roughly like $\alpha_{\gamma_{nD}} \cong 2.85/L$ as shown in Figure 7 b), where L is expressed in nm.

It can be shown that the minimum noise factor and input-referred noise resistance of a single common source stage are given by

$$F_{min} \cong 1 + 2\omega C_{GS} \cdot \frac{\gamma}{G_m} \cdot \sqrt{\frac{\gamma}{\beta} \cdot (1 - c^2)} \text{ and } R_n \cong \frac{\gamma}{G_m}, \tag{16}$$

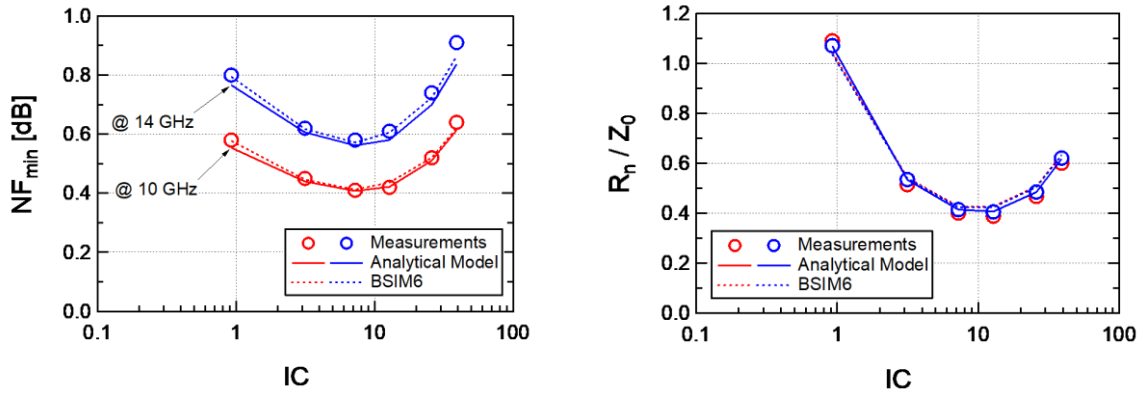
where $\beta = 1/(5n)$ in SI and $\beta = 4/(15n)$ in WI. The ratio γ/G_m and hence R_n and F_{min} find a minimum at the upper limit of MI as shown in Figure 8.



a) *Noise excess factor γ vs. IC for short-channel devices from various technologies*

b) *Scaling of the $\alpha_{\gamma_{nD}}$ parameter.*

Figure 7: Noise excess factor γ vs. IC for short-channel devices from various technologies.



a) *Minimum noise figure measured at RT for a 40 nm technology.*

b) *Input-referred noise resistance normalized to 50 Ω measure at RT for a 40 nm technology.*

Figure 8: Minimum noise figure and input-referred noise resistance vs. IC measured at RT on a 40nm technology.

It is unclear how these RF noise parameters will behave at cryogenic temperatures. The white noise, whether it is thermal noise or shot noise, will be measured at cryogenic temperature and at low frequency using an on-chip dedicated measurement circuit designed under WP4.

2.3 EKV Parameter Extraction Tool

The EKV parameters can be extracted manually following the procedure described in [10]. However, the manual extraction is quite time-consuming and requires a good understanding of the simplified EKV model. For this reason, a parameter extraction tool has been developed that will make the sEKV model and the related design methodology more widely available for analogue circuit designers. The tool efficiently extracts the EKV parameters from the I_D-V_G transfer characteristics, which are either measured or generated from an existing PDK.

The concept of the extraction methodology is initially based on the extraction methodology presented in [10]. However, the process has been made fully automatic by the use of performant optimization techniques. The latter are based on non-linear regression, which looks for the local minimum error. For further information, the mathematical optimization algorithm used in the tool is taken from the *Python Scipy* library. In general, optimization functions require initial guesses and boundaries, depending on which algorithm is used in the optimizer. Accordingly, the results obtained from the optimizer

depend on how initial guesses and boundaries are specified. In fact, several local minima can be found in the defined boundaries. Even an unphysical set of initial guess is able to fit data mathematically with low error, resulting in extracted parameters that are far from the expected physical values.

The numerical computation issue mentioned above has often been observed for parameters I_{spec} and λ_c when the optimization technique is directly applied to a given data including the effect velocity saturation (basically short-channel devices). This is due to the fact that the ratio of I_{spec} over λ_c is constant and given by

$$\frac{I_{spec}}{\lambda_c} = nWC_{ox}v_{sat}U_T, \tag{17}$$

This means that I_{spec} and λ_c are trying to compensate each other to fit the input data with low residual error. This problem can be circumvented by extracting I_{spec} from the WI regime, where the diffusion dominates the transport mechanism. The transconductance G_m in the WI and saturation is given by

$$G_m = \frac{1}{nU_T} \cdot I_{spec} \cdot e^{\frac{V_G - V_{T0}}{nU_T}}. \tag{18}$$

Taking the natural logarithm on both sides results in a linear function given by

$$ln(G_m) = \frac{V_G - V_{T0}}{nU_T} + ln\left(\frac{I_{spec}}{nU_T}\right). \tag{19}$$

From (19), we see that I_{spec} can be computed from the intercept of the $ln(G_m)$ versus $V_G - V_{T0}$ regression line. However, the threshold voltage V_{T0} has to be known first.

Therefore, a four-step extraction procedure shown in Figure 9 is introduced. From step 1 (Sec. 2.3.1) to step 3 (Sec. 2.3.3), the initial extraction method presented in [10] is used and optimization are used to calculate the precise V_{T0} automatically, which is needed in (19) to avoid the issues caused by numerical computation (see Sec. 2.3.4). The proposed four-step procedure is presented in more details in the following subsections.

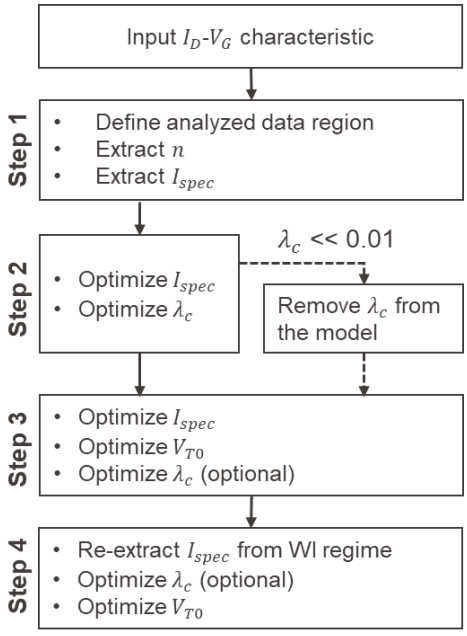


Figure 9: Four-step procedure used in the proposed extraction methodology.

2.3.1 The automated EKV parameters extraction methodology: Step 1

Compact models of advanced CMOS technologies need hundreds of parameters to accurately simulate the transistor behaviour accounting for all the short-channel effects. On the contrary, sEKV requires only four parameters to model the I_D-V_G transfer characteristics. However, the model ignores mobility reduction due to the vertical field and most of the SCEs, except velocity saturation. Those effects are observed at rather high current in the SI regime and should be separated from the entire V_G sweeping. Hence, this step aims to determine proper data region based on WI and SI asymptotes from the curve $I_D/(G_m U_T)$ versus I_D, which is labelled as the analysed data (blue cross marker) as shown in Figure 10 a) and Figure 11 a); $I_D/(G_m U_T)$ converges to a plateau in the WI regime, which allows us to define the slope factor n. The asymptote in SI regime, represented by the blue dash line in Figure 10 a) and Figure 11 a), can be expressed as

$$\log\left(\frac{I_D}{G_m U_T}\right)\Big|_{SI,saturation} = \begin{cases} \frac{1}{2}\log(I_D) + \log\left(\frac{n}{I_{spec}}\right) \ (without\ VS) \\ \log(I_D) + \log\left(\frac{n}{\lambda_c I_{spec}}\right) \ (with\ VS) \end{cases}. \quad (20)$$

It is clear that the slope of the asymptotes in the SI regime for long- and short-channel transistors are 0.5 and 1.0, respectively.

To automatically extract n from the plateau shown in Figure 10 a) and Figure 11 a), some filtering techniques, such as the polynomial and Savitzky-Golay filter [21], are used to lower the influence of fluctuations. The green dash line represents the filtering curves in Figure 10 a) and Figure 11 a). The n is then defined by the local minimum of the filtered curve, in which the lower boundary of analysed data region is also determined. Since exclusive phenomenon in SI regime shows degradation in transconductance, it results in the rising up $1/(G_m U_T)$. This implies that the slope of theoretical SI asymptote (Eq. (20)) is no longer valid, especially for short-channel devices. Consequently, to avoid comprising those unmodeled behaviours, the upper boundary of the analysed data is defined by where the theoretical SI asymptote is reached. Nonetheless, I_{spec} is subsequently extracted from the intersection of an extended line from n plateau and SI asymptote.

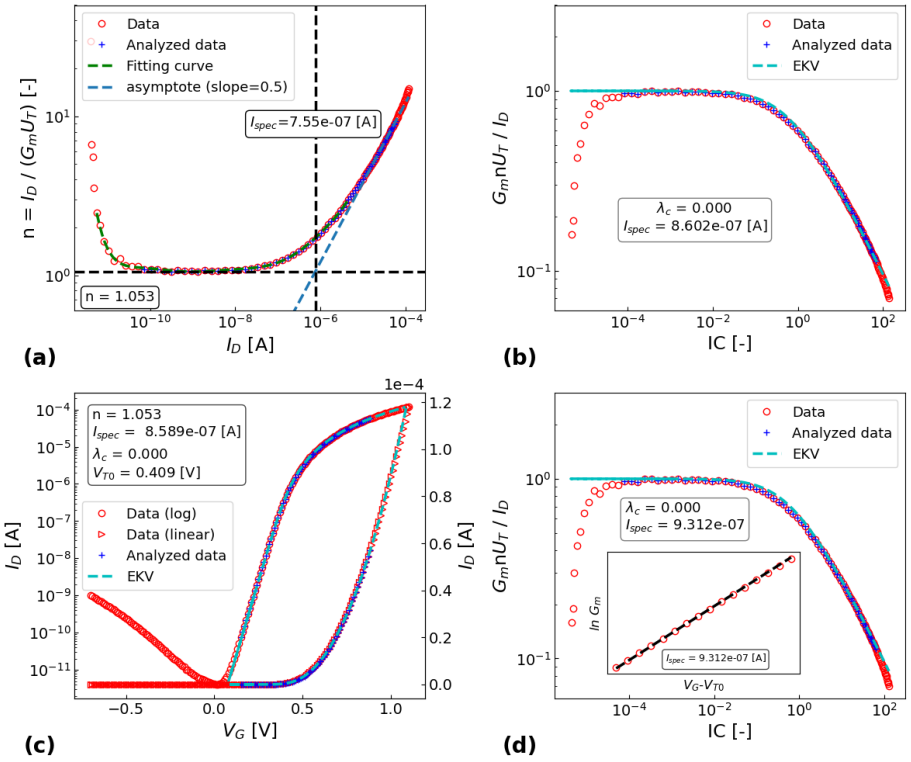


Figure 10: Automated EKV extraction process of n-type FDSOI with W/L = 1 um/1 um and $V_B = 0$. (a) Definition of analyzed data based on WI & SI asymptotes of the curve of $I_D/(G_m U_T)$ vs. I_D (Step 1). (b) Extraction of I_{spec} and λ_c from current efficiency (Step 2). (c) V_{T0} extraction from transfer characteristic (Step 3). (d) Re-extraction of EKV parameters based on re-defining I_{spec} in WI regime (Step4).

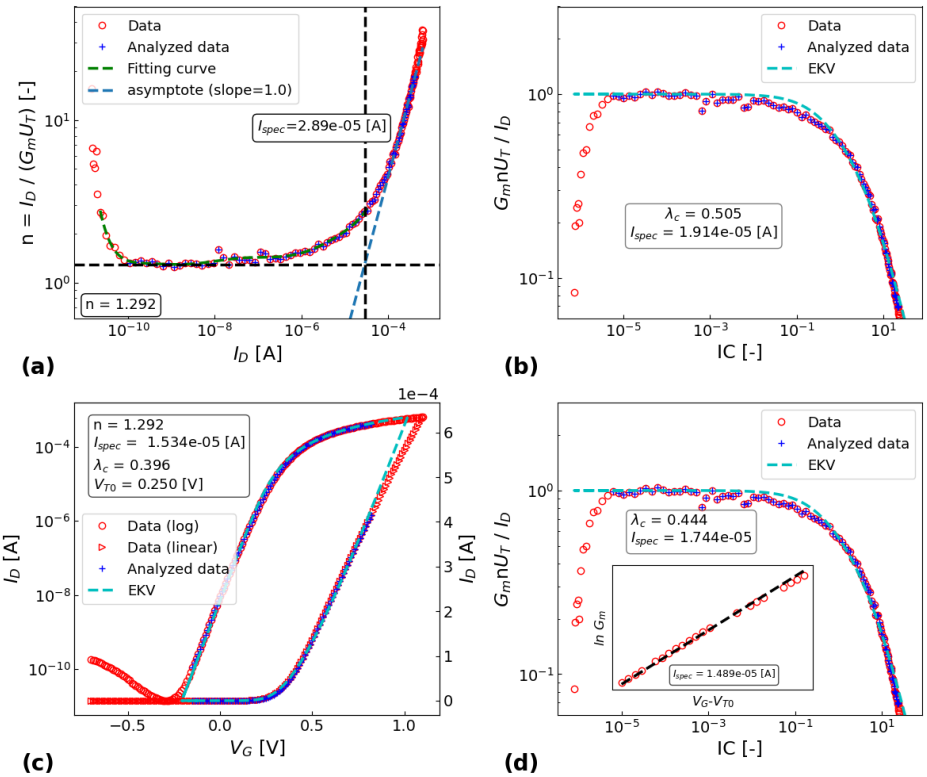


Figure 11: Automated EKV extraction process of n-type FDSOI with W/L = 0.5 um/18 nm and $V_B = 0$. (a) Definition of analyzed data based on WI & SI asymptotes of the curve of $I_D/(G_m U_T)$ vs. I_D (Step 1). (b) Extraction of I_{spec} and λ_c from current efficiency (Step 2). (c) V_{T0} extraction from transfer characteristic (Step 3). (d) Re-extraction of EKV parameters based on re-defining I_{spec} in WI regime (Step4).

2.3.2 The automated EKV parameters extraction methodology: Step 2

Thus far, n and I_{spec} were obtained from Sec. 2.3.1. It is important to note that a slight deviation in the asymptotes' interception leads to a significant change in the I_{spec} value. Moreover, according to (20*)*, the interception of an asymptote in the SI regime is related to λ_c if velocity saturation is present. Hence, the I_{spec} extracted from Sec. 2.3.1 cannot be regarded as its eventual value, but needs to be re-defined in Sec. 2.3.4. In this section, the inaccurate I_{spec} can be still used as the initial guess in the following optimizing process to obtain λ_c.

As stated by (10), the current efficiency is a function of λ_c and IC. Parameter λ_c could be efficiently iterated by the use of optimization on (10) with I_{spec} obtained from Sec. 2.3.1 as the initial guess. Besides, a reasonable initial guess for λ_c is set to 0.2 by default. Thereby, the outcomes of numerical computation are shown in Figure 10 b) and Figure 11 b) for long- and short-channel devices, respectively. Note that, as expected, λ_c drops to zero for the long-channel transistor due to negligible velocity saturation effect. On the contrary, λ_c rises up to about 0.51 due to the presence of velocity saturation in the 18 nm-long channel. Nonetheless, the fraction of I_{spec} over λ_c is independent of V_G, as stated by (17). Hence, Eq. (10) is true for several pairs of I_{spec} and λ_c which might have a low-error mathematical fitting on the input data but could be without any physical meaning, which is the numerical computation issue addressed in Sec. 2.3. Even though I_{spec} and λ_c optimized from this step might not be exact values, the main goal in the section is to clarify the influence of velocity saturation. If λ_c is small enough to be negligible, meaning that I_D- V_G curve follows quadratic model, the rest of steps would exclude λ_c from the sEKV model and set it to be zero.

2.3.3 The automated EKV parameters extraction methodology: Step 3

Until now, n is extracted from Sec. 2.3.1, I_{spec} and λ_c are optimized from Sec. 2.3.2. The last EKV parameters V_{T0} can be straightforwardly optimized from I_D-V_G transfer characteristics. According to (6), the threshold voltage V_{T0} can be considered as a parameter that shifts the I_D-V_G curve horizontally, since it is not related to its curvature. If n, I_{spec}, and λ_c provide low-deviation fitting on the input data curvature, V_{T0} could be therefore optimized as rigorously as possible.

In the optimization process, only n is fixed, and the other EKV parameters are kept floating during the iterative process. Results of the long- and short-channel transistors are shown in Figure 10 c) and Figure 11 c), respectively.

At this point, the sEKV model nicely fits the input data over about seven orders of magnitude of current. There are two points worth to be noted:

1. some discrepancy between the input data and the model is observed in the SI regime, which is due to the exclusion of mobility reduction due to the vertical field and/or access resistance. Figure 11 c) shows a significant deviation in the SI regime as the presence of relatively strong SCEs.
2. In the short-channel device, the decrease of I_{spec} and λ_c is noticeable from Figure 11 b) to Figure 11 c), but the ratio I_{spec}/λ_c remains at about 38 μA in both cases. Even though these two sets of parameters are coming from different curves, it tells us again that a low fitting error does not imply that the numerically optimized parameter follows its meaning in physics.

Therefore, an additional step is required to solve the issue of numerical computation properly.

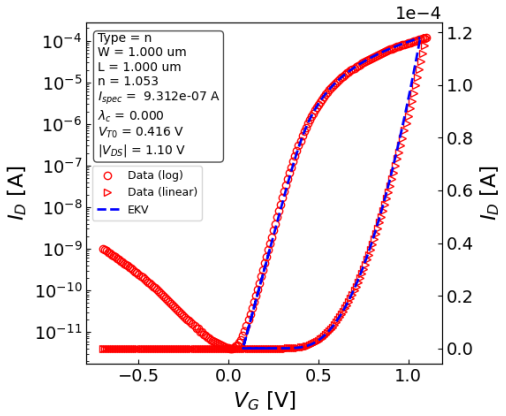
2.3.4 The automated EKV parameters extraction methodology: Step 4

As discussed in Sec. 2.3, V_{T0} is needed for re-extracting I_{spec} by following (19). The curves of $ln\, G_m$ versus $V_G - V_{T0}$ are shown in the subplot of Figure 10 d) and Figure 11 d). Once I_{spec} is obtained, λ_c can be optimized as well by redoing Step 2 (Sec. 2.3.2) but with a fixed or low-tolerated I_{spec}. It should be pointed out that the tolerance on the specific current has been experimentally defined within $\pm$10 mV range with respect to the threshold voltage through (19) for the 22 nm FDSOI technology (Global Foundries) to compensate for the presence of Drain Induced Barrier Lowering (DIBL). As shown in Figure 11 d), the I_{spec} value in the subplot is lower than the one in the main plot due to the use of threshold voltage tolerance.

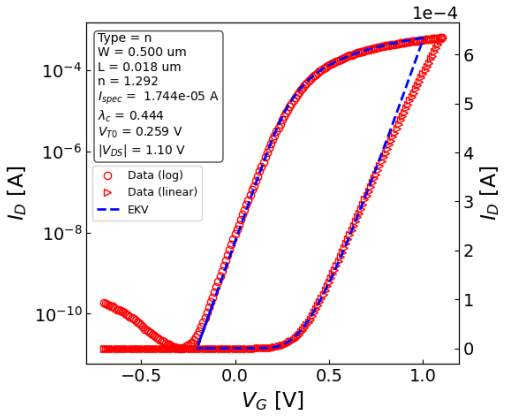
Ultimately, V_{T0} is re-optimized by similarly following Step 3 (Sec. 2.3.3) while keeping other EKV parameters fixed. The final results coming from the automated extraction platform for n- and p-type FDSOI transistors are shown in Figure 12 and Figure 13, respectively. The design-oriented EKV model with extracted parameters shows a nice agreement between the measured transfer characteristics in both the long- and the short-channel cases.

As shown in Figure 14, the automated extraction tool potentially can also extract the EKV parameters from the data of FDSOI transistors measured at cryogenic temperature (actually at 2.95 K).

The use of optimization allows the parameters extraction process to be automated and robust. Besides, the proposed methodology does not require operators to tune the initial guesses of the optimizer manually. It is worth noting that the tool takes only a few seconds to complete the whole extraction process. It drastically reduces the time spent on extraction in comparison with manual operation.

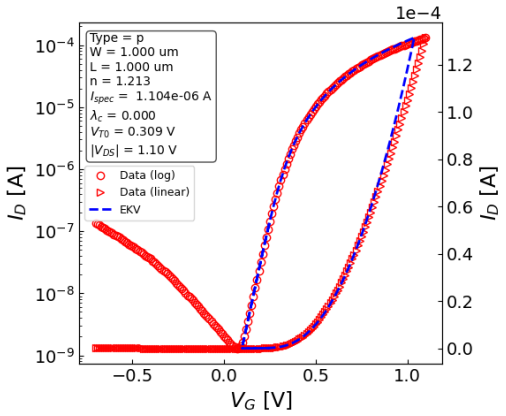


(a) Extraction result of n-type long-channel FDSOI (W/L = 1 um/1 um, $V_B = 0$)

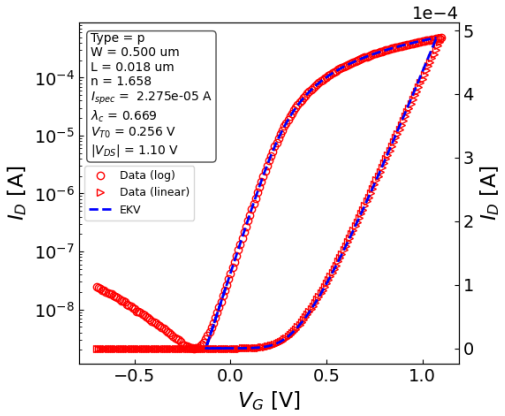


(b) Extraction result of n-type short-channel FDSOI (W/L = 0.5 um/18 nm, $V_B = 0$)

Figure 12: Final outputs from the automated EKV parameters extraction platform for n-type FDSOI transistors.



(a) Extraction result of p-type long-channel FDSOI (W/L = 1 um/1 um, $V_B = 0$)



(b) Extraction result of p-type short-channel FDSOI (W/L = 0.5 um/18 nm, $V_B = 0$)

Figure 13: Final outputs from the automated EKV parameters extraction platform for p-type FDSOI transistors.

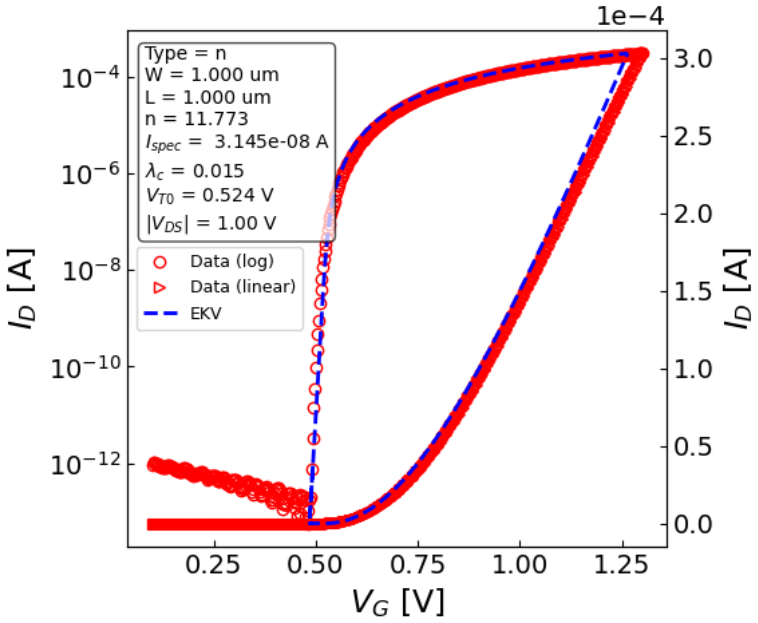


Figure 14: I_D-V_G transfer characteristic and EKV extraction results of n-type FDSOI transistor with W/L = 1 um/1 um operating at 2.95 K and $V_B = 0$.

3 Poisson-Schrödinger simulation of inversion charge and associated analytical modelling of FDSOI MOSFET

Research on cryogenic electronics has started decades ago [22] with application in the spatial field. Nowadays, the emergence of quantum computing restores the interest for cryogenic applications. Indeed, in order to control the Qubit (which ideally operates around 0K), a nearby electronics operating at deep cryogenic temperatures (between 0 and 4 K) is mandatory [23]. Early demonstrations of quantum computers have illustrated their potential when several qubits are operating, and cryo-electronics is necessary to assure the control and read-out of such a large number of qubits. FDSOI cryo-CMOS is a promising candidate to this end due to its superior electrostatic control, no channel doping needed, higher performance and low power consumption.

It should be noted that many works have been done before on Poisson-Schrödinger simulation in bulk or FDSOI MOSFETs at room or low temperatures [24] [25] [26] but not down to very low temperatures (<2K). Besides, CEA-LETI has developed a physics-based compact model dedicated to FDSOI technology called LETI-UTSOI [27]. However, this model has not been developed for deep cryogenic temperature operation. In this section, we demonstrate for the first time Poisson-Schrödinger simulations of carrier charge in FDSOI structure down to 0K. Then, we propose the first charge analytical model for FDSOI devices with back biasing operation at deep cryogenic conditions.

3.1 Simulation methodology

The Poisson-Schrödinger (PS) solver is based on a Python program solving self-consistently the Schrödinger and Poisson equations recalled below:

$$H(\psi) = E.\psi \tag{21}$$

$$\nabla(\varepsilon_r \nabla V) = -\frac{q.n(x)}{\varepsilon_0}. \tag{22}$$

with H the hamiltonian, E the system energy, Ψ the electron wave function, $\varepsilon 0$ and εr the vacuum and relative silicon permittivity.

Once, the electrical potential V and the subband energies Ei,j and wave functions Ψi,j are computed in a FDSOI structure for various front and back gate voltages, the electron density is obtained after summing the different valleys and subband contributions as:

$$n(x) = \sum_{j=1}^{2} \sum_{i=1}^{i\max} g_j A_{2dj} kT.\psi_{i,j}^2(x).F_0\left(\frac{Ef - E_{i,j}}{kT}\right) \tag{23}$$

with kT thermal energy, F_0 the zero-order Fermi-Dirac integral function, Ef Fermi level, Ei,j subband energy for valley j and level i, gj valley degeneracy, A2dj 2D density of states for valley j.

In order to simulate the PS equations down to very low temperature (1K), special truncation care has been taken to avoid numerical overload in the F_0 Fermi integral function accounting for Fermi-Dirac statistics. PS simulations were even made possible at 0K by replacing the F_0 Fermi-Dirac integral function by a Heaviside function, emulating the fully degenerate metallic statistics.

3.2 PS simulation results and discussion

Typical FDSOI structure used for PS simulation is shown in Figure 15, illustrating the band diagram across the stack and the electron density profile in the channel obtained from PS solution at T=4K for a given bias condition. Without loss of generality, midgap gates are considered in this study.

Figure 16 shows the variations of the inversion charge Qi in the Si channel as a function of front gate voltage Vg with Vb=+3V, obtained from PS simulations for various temperatures T=0-60K. Note the strong increase of the subthreshold slope with temperature lowering, becoming ideally infinite at T=0K, which is an appealing consequence of transistors functioning at such low temperatures.

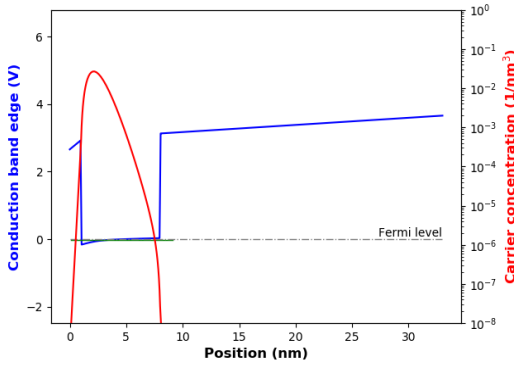


Figure 15: Typical band diagram and electron distribution from PS simulation for a FDSOI structure (V_g=1V, t_{ox}=1nm, t_{box}=25nm, t_{si}=7nm,V_b=0V, T=4K.

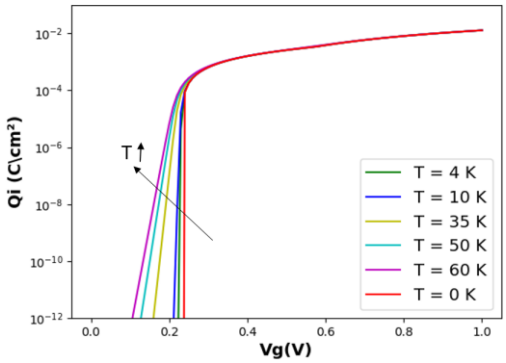


Figure 16: Qi(Vg) for different temperatures (tox=1nm, tbox=25nm, tsi=7nm, Vb=+3V).

Figure 17 better illustrates the channel inversion charge control by field effect via the variations of the gate-to-channel capacitance Cgc(Vg)=dQi/dVg with front gate voltage for various back gate bias, revealing the early onset of back inversion channel followed by the front channel opening for Vb=+3V. This feature of Cgc(Vg) curve clearly reveals the through-the-silicon coupling between the front gate and the back channel inversion layer with a lower capacitance. The influence of temperature on the Cgc(Vg) curves is displayed in Figure 18, clearly showing the rounding of the curves with temperature increase above T=10K. Note that these simulation results well agree with experimental ones shown in [28].

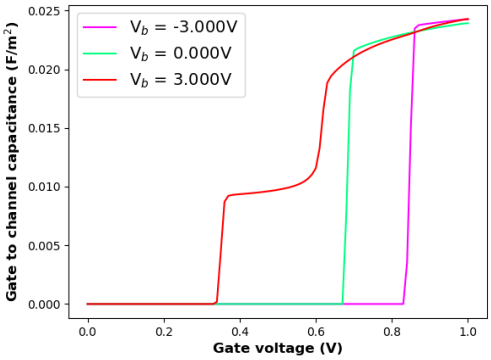


Figure 17: Cgc(Vg) curves for different back bias (tox=1nm, tbox=25nm, tsi=10nm, T=4K).

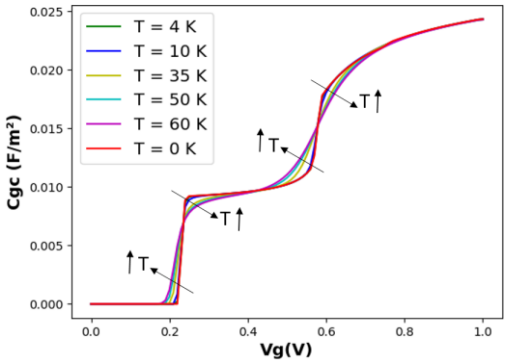


Figure 18: $C_{gc}(V_g)$ curves for different temperatures (t_{ox}=1nm, t_{box}=25nm, t_{si}=10nm,V_b=+3V).

Moreover, *Figure 19* reports the impact of the silicon channel thickness on the Cgc(Vg) characteristics at T=4K and Vb=+3V, demonstrating a delayed and stronger through-the-silicon back channel coupling as the silicon film thickness is reduced. Note also the larger capacitance shoulder effect before front channel opening for tsi=7nm, which can be explained by the higher carrier profile overlap between the back and front interface electron distributions as tsi is reduced (see *Figure 20*). Instead, for larger tsi values, the overlap is decreased, so that front and back channels are better separated.

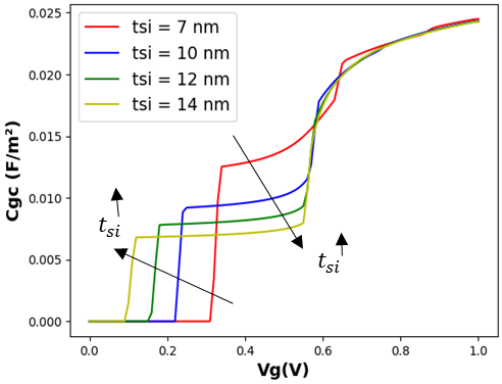


Figure 19: Cgc(Vg) curves for different channel thickness (tox=1nm, tbox=25nm, T=4K, Vb=+3V).

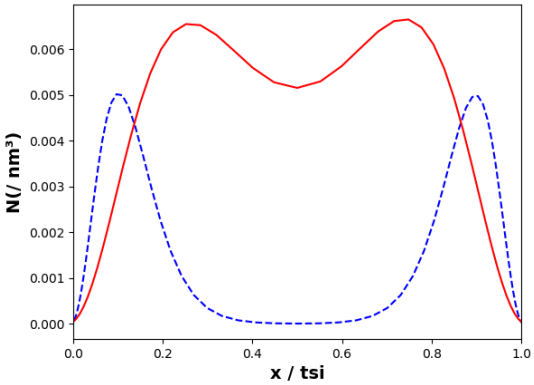


Figure 20: Electron distribution in the channel (tox=1nm, tbox=25nm, tsi=7nm for red line and tsi = 16 nm for blue dashed line, T=4K, Vg=0.73V, Vb=+3V).

3.3 Airy function based analytical model

Based on the PS simulation results, an analytical model has been developed considering that front and back channel charges can be calculated separately at each interface on a single subband, whose energy level is given by the triangular potential well approximation within Airy's function approach [29]. The coupling is achieved by the mean of the silicon channel capacitance Csi and the charge sheet approximation along with Fermi-Dirac statistics is chosen to describe the system.

In this context, the charge conservation equations at front and back interfaces are written as:

$$V_g = V_{fb} + V_{s1} + \frac{qN_{i1}}{C_{ox}} + \frac{C_{si}.(V_{s1} - V_{s2})}{C_{ox}} \tag{24}$$

$$V_b = V_{fb} + V_{s2} + \frac{qN_{i2}}{C_{box}} + \frac{C_{si}.(V_{s2} - V_{s1})}{C_{box}} \tag{25}$$

with front and back interface 2D carrier density given by,

$$N_{inv1,2} = A_{2d}.F_0\left[\frac{V_{s1,2} - V_0 - \Delta V(F_{1,2})}{kT}\right] \tag{26}$$

where Vs1 (Vs2) is the front (back) interface surface potential, Cox (Cbox) the front (back) oxide capacitance, Csi the silicon film capacitance. The front and back electric field are given by:

$$F_1 = (V_g - V_{s1} - V_{fb})/3t_{ox}\,. \tag{27}$$

$$F_2 = (V_b - V_{s2} - V_{fb})/3t_{box} \tag{28}$$

with Airy's subband potential shift $\Delta V(F) = K.|F + F_0|^{2/3}$ with K=1.75x10^{-5}V$^{1/3}$cm$^{2/3}$. Note also that, since the structural confinement becomes dominant when the electrical field approaches zero, a field offset F0 is added to the electric field in Eqs (27)(28), in order to account for the silicon film flat band quantum confinement. This offset field is given by:

$$F_0 = \frac{h^2}{8m_c q.t_{si}} \tag{29}$$

with mc=0.918.m0 is the electron confinement effective mass in the 2 direction.

Typical Qi(Vg), Vs(Vg) and Cgc(Vg) characteristics obtained by this simple Airy-based analytical model are compared in Figure 21 to Figure 24 to the PS simulation results, showing an overall good agree-

ment between them, especially for not too small silicon thickness where wave function overlap between front and back interface is not important. The results point out the main set of implicit equations to be solved for cryogenic analytical mode.

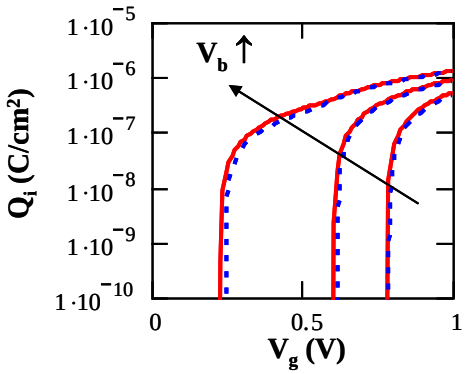


Figure 21: $Q_i(V_g)$ curves obtained from PS simulations (solid lines) and analytical modeling (dashed lines) for various V_b=-3, 0, +3V (T=4K, t_{ox}=1nm, t_{box}=25nm, t_{si}=10nm).

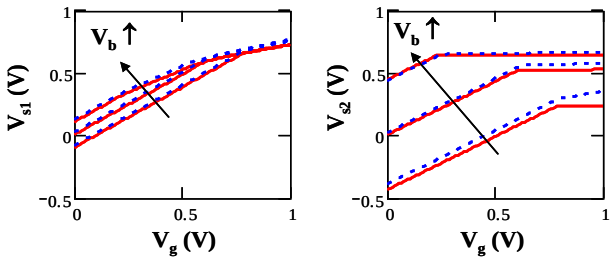


Figure 22: Comparison of Vs1(Vg) and Vs2(Vg) curves as obtained from PS simulations (solid lines) and analytical modeling (dashed lines) for various Vb=-3, 0, +3V (T=4K, tox=1nm, tbox=25nm, tsi=10nm).

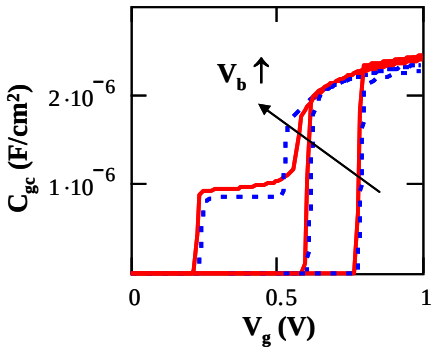


Figure 23: $C_{gc}(V_g)$ curves obtained from PS simulations (solid lines) and analytical modeling (dashed lines) for various parameters V_b=-3, 0, +3V (T=4K, t_{ox}=1nm, t_{box}=25nm, t_{si}=10nm).

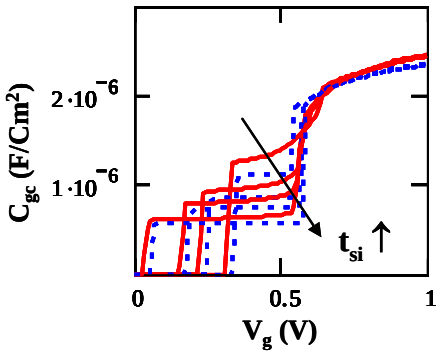


Figure 24: $C_{gc}(V_g)$ curves obtained from PS simulations (solid lines) and analytical modeling (dashed lines) : for various t_{si}=7, 10, 12, 16 nm (T=4K, t_{ox}=1nm, t_{box}=25nm, V_b=+3V).

4 Transistor models for HEMTs suitable for the design of ultra-low noise amplifiers at ambient temperatures of 300 K and 10 K

In this Section, a highly scalable small-signal modelling approach for High Electron Mobility Transistors (HEMTs) is introduced which is able to predict the small-signal response of HEMTs at temperatures continuously ranging from room temperature down to cryogenic temperatures as cold as 10 K. The design of cryogenic low-noise amplifiers (LNAs) relies on accurate small-signal and noise models to optimize the circuit performance at cryogenic conditions where the electrical properties of the active device changes compared to room temperature operation. Furthermore, accurate modelling is necessary to minimize design-iterations, which results in a significant time and cost reduction. Especially cryogenic testing adds a significant effort per design iteration and should be kept at an absolute minimum. The geometry of a HEMT is a key design-parameter for every monolithic microwave integrated circuit (MMIC) both at room temperature and at cryogenic conditions. The geometry is accessible by the designer in terms of the gate-finger number and the gate-width (in the following given as: absolute gate width W_g = finger number n_F × gate width per finger W_F). Precise modelling of all possible geometries is mandatory for state-of-the-art MMIC design, which demands for highly scalable model topologies. Furthermore, the choice of the optimal bias point affects the circuit performance especially under cryogenic conditions, where a trade-off between power dissipation heating the device and a high gain bias point is favourable. Therefore, the model shall cover a wide region of bias points. As different applications demand for different frequencies, the model needs to be able to describe a frequency range as broad as possible. Furthermore, the continuous description of different temperatures between 10 K and 300 K is desirable since it also allows for a circuit design for other upcoming cryo-applications (e.g. remote earth observation missions, space communication, …) that utilize cooling systems that are not capable to reach deep cryogenic temperatures, as for example liquid nitrogen cryostats.

Scalable small-signal models are well studied at room temperature [30], [31], [32], [33], [34], [35] where scalability and coverage of a wide frequency range have been increased successively. First investigations of continuous temperature dependency have been published for 100 nm InGaAs HEMTs on InP substrate, but no scalability at different temperature levels has been demonstrated so far [36], [37]. The model presented in this report combines high scalability, a broad frequency range and the ability to continuously describe the small-signal properties at temperatures between 10 K and 300 K. These outstanding model properties will allow for the inclusion of an accurate noise model both at room and at cryogenic temperatures in the next step.

The model topology presented is extracted based on Fraunhofer IAF's 50 nm metamorphic HEMT technology [38], which is an excellent candidate for ultra-low noise amplification both at room temperature and at cryogenic conditions [35], [39], [40].

4.1 Distributed Small-Signal Model Topology

The model topology that is extended for temperature dependent operation down to 10 K bases on the distributed approach presented in [34]. Today's RF models utilize an equivalent circuit to describe the transistor in terms of its active, intrinsic components and its parasitic, extrinsic circuit components. In contrast to widely used shell-modelling topologies (e.g. [30], [31], [32], [36]) that describe the extrinsic elements of the transistor in a way that they fit the structure of a three-port best, the distributed approach closely orientates at the actual transistor layout. This has the advantage that realistic modelling of coupling effects up to very high frequencies is possible while linear scaling rules are preserved. Figure 25 shows how the distributed model divides the transistor structure according to its layout at the example of a four-finger common-source transistor and Figure 26 shows the corresponding block diagram describing how the parts are interconnected.

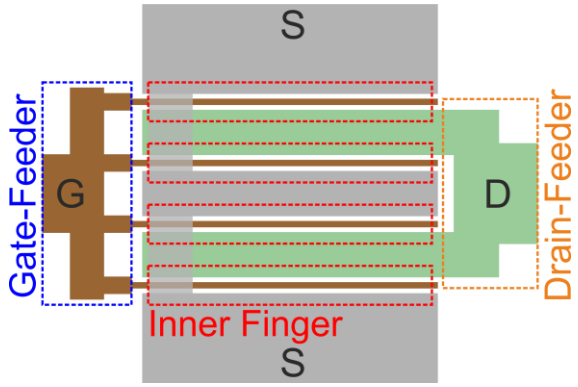


Figure 25: Four finger common-source HEMT layout (top-view). Dashed boxes mark how the model divides the transistor structure into parts. Red denotes the gate-finger area including all three transistor electrodes, blue marks the gate-feeder and orange the drain-feeder network.

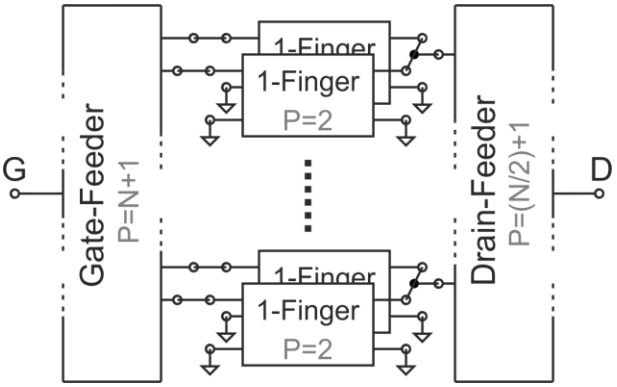


Figure 26: Block diagram of the distributed model showing the interconnection scheme of the different transistor sub-parts. Grey numbers denote the port numbers of the sub-parts during interconnection.

The majority of (parasitic) coupling is found in the area of the of the gate finger (marked in red in Figure 25) where the metal electrodes are placed very close to each other. Accurate modelling of this region is therefore of tremendous importance to achieve widest scalability and coverage of frequency range. Each finger region is modelled by an interconnection of ten six-port elements each describing a slice of a tenth of the unit gate width of the overall finger region. The setup as six-ports follows naturally from the layout of the transistor finger area since each electrode (gate, drain and source) has an input-sided and output-sided connection. The equivalent circuit modelling the extrinsic finger area is shown in Figure 27. The parameter set per unit length is equal for the different finger-area sub-parts and all elements scale linear with the width of the corresponding finger-sub-part. The distributed setup of the finger region enhances the scalability in terms of unit gate width since also very long finger elements can be described up to high frequencies, where the size of the structure cannot be considered short compared to the wavelength anymore.

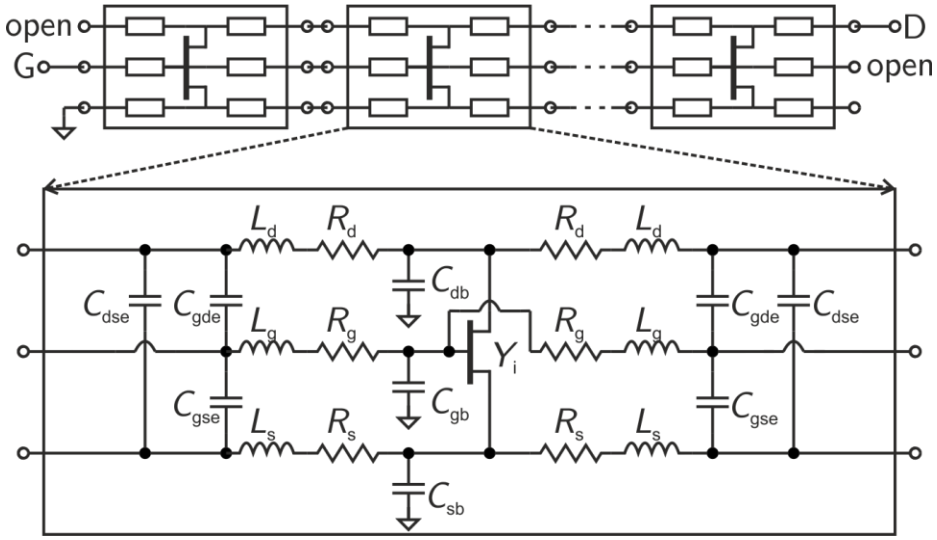


Figure 27: Distributed modelling of the transistor finger area including the three transistor electrodes. On top the interconnection of the six-ports that model slices of the finger region are shown, while on the bottom the equivalent circuit representation of these six-ports is shown. The lumped elements model the passive part of the HEMT and the transistor symbol Y_i marks where the active, intrinsic circuit is connected.

Every finger-area sub-part contains one intrinsic core that scales linearly with the width that is represented by the sub-part. Figure 28 shows the equivalent circuit of the intrinsic HEMT.

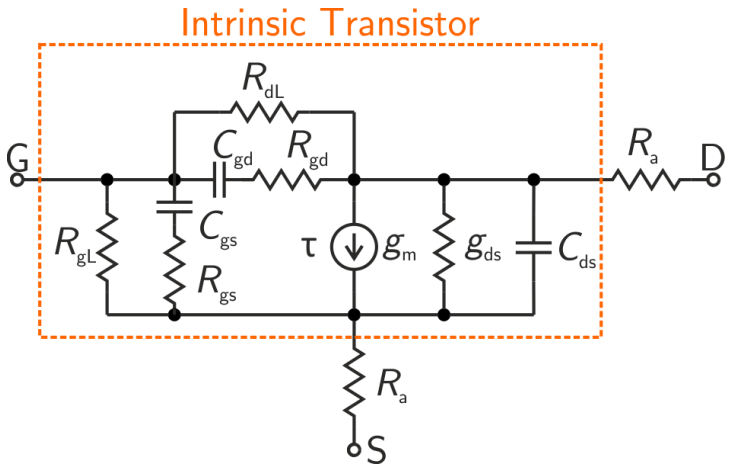


Figure 28: Equivalent circuit representation of the intrinsic transistor. One intrinsic circuit is contained in each finger sub-part (replaced by the transistor symbol in Figure 27).

Besides the scaling according to the gate width, the intrinsic elements are bias dependent. The bias dependency is modelled by first to third order Taylor series depending on the drain current and the drain voltage. The model parameters have been extracted using a dedicated simplex algorithm minimizing the root-mean-square deviation between the model output and a data set of S-parameter measurements. A bias region ranging from 50 mA/mm to 400 mA/mm drain current and from 0.3 V to 1.0 V drain voltage is covered by the model. This region includes all bias points typically used in room temperature applications. The scalability and the broadband response of the proposed model is verified at on-wafer S-parameter measurements from 10 MHz to 150 GHz at various transistor geometries. Figure 29 compares on-wafer measurements of HEMTs with various gate width including extremely small (W_g = 10 µm) and extremely large (W_g = 480 µm) devices. Furthermore, transistor finger numbers between 2 and 8 are verified, which include all finger numbers supported by the technology. Extremely short finger devices (W_F = 5 µm) and extremely long finger devices (W_F = 100 µm) are correctly described. A scaling ratio of 48 is achieved in terms of absolute gate width and the ratio of the longest finger device to the shortest finger device, that have been modelled, is 20, proofing the high scalability of the model. The measurements and the model are compared in two different bias points, which demonstrates the feature to use the model at arbitrary bias conditions.

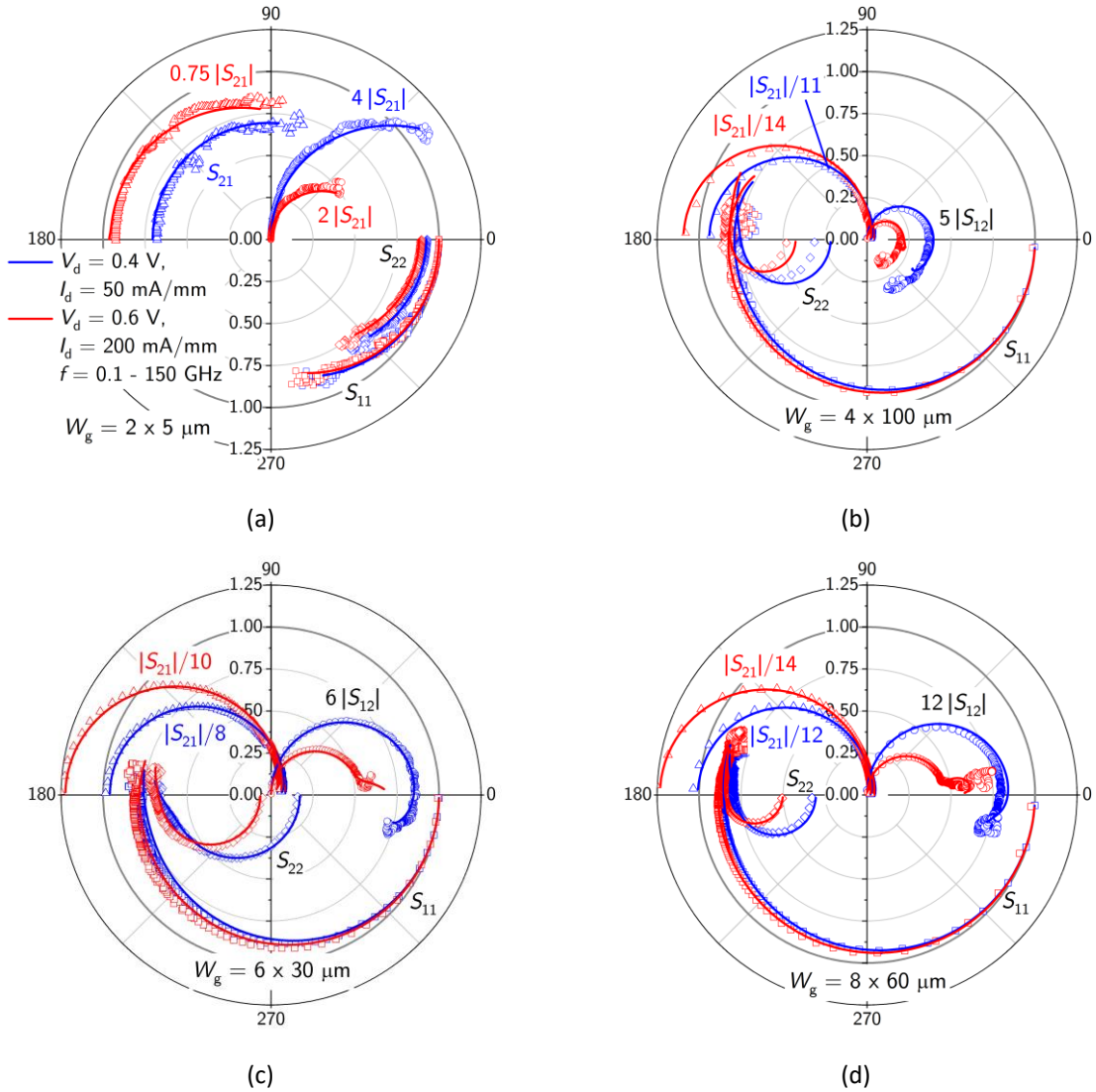


Figure 29: Room temperature on-wafer S-parameter measurements (symbols: squares S_{11}, circles S_{12}, triangles S_{21} and diamonds S_{22}) between 0.01 GHz and 150 GHz of 50 nm mHEMTs compared to the modelled S-parameters (lines). Common-source HEMTs with an absolute gate-width of W_g = 2 × 5 µm (a), W_g = 4 × 100 µm (b), W_g = 6 × 30 µm (c) and W_g = 8 × 60 µm biased at V_d = 0.4 V, I_d = 50 mA/mm (blue) and V_d = 0.6 V, I_d = 200 mA/mm (red) are shown.

4.2 Temperature Dependent Small-Signal Model Including Cryogenic Operation

The room temperature small-signal model forms the basis for the temperature dependent small-signal model. The temperature dependency of all model parameters is extracted to obtain a fully temperature scalable model. The extraction is based upon DC and S-parameter measurements at different temperatures between 10 K and 300 K. The measurements have been taken in a Lakeshore cryogenic probe station utilizing a closed-cycle helium refrigerator to cool the devices-under-test (DUTs) as cool as 5 K. The DUTs are glued with silver-epoxy onto a gold-plated copper carrier to ensure best thermal coupling to the cooling finger. Thermal sensors in combination with an electronic PID control ensure that the DUTs are at the desired temperature during testing. Figure 30 shows a picture of the sample holder with DUTs attached in the cryogenic probe station.

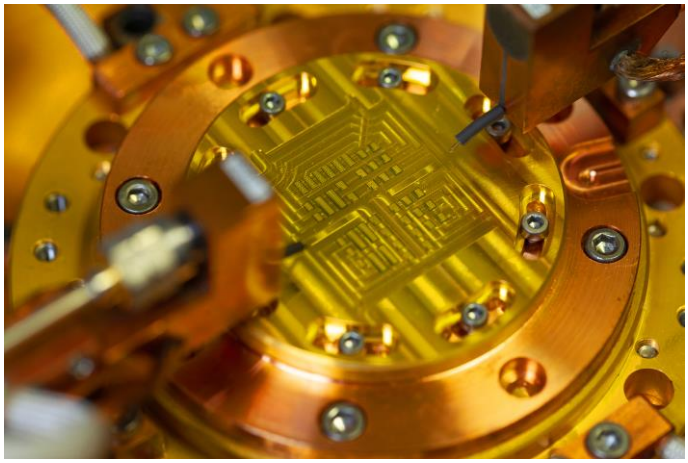


Figure 30: Close-up view on the sample-holder containing the glued DUTs in the cryo-chamber.

Precise modelling of the resistive elements of the extrinsic circuit is of special importance since thermal noise will be generated in these elements in a later noise model. The most important resistive element is the gate-line resistance, which has a considerably high resistance due to its small cross-section. The thermal dependency of the gate-line resistance is evaluated by four-wire measurements of gate-line meander test-structures at several temperatures. Figure 31 shows the measured gate-line resistance (symbols) per unit-gate width dependent on the temperature and the modelled temperature dependency (line). With decreasing temperature, the gate-line resistance decreases linearly which is believed to originate from reduced phonon scattering in the gold that forms the gate line at lower temperatures. Below 75 K the decrease starts to settle until no further improvement is achieved (below approximately 25 K), which is an evidence for impurity scattering in the gold.

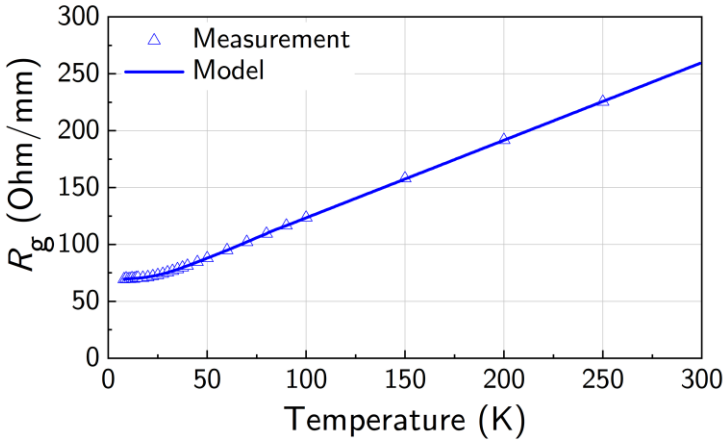


Figure 31: Measured (symbols) and modelled (line) gate line resistance dependent on the temperature.

The ohmic contact resistance and the semiconductor sheet resistance, which both form the connection of the active HEMT with the drain and source electrodes, have a significant influence on the small-signal properties of the device. The temperature dependency of both is evaluated by four-wire transfer length measurements at different temperatures utilizing dedicated test structures. Figure 32 shows the temperature dependency of the sheet resistance (blue) and the contact resistance (red). The semiconductor sheet resistance decreases linearly with temperature until the decrease settles below approximately 75 K. Increased carrier mobility motivates the linear resistance decrease with temperature and impurity scattering is believed to cause the saturation behaviour at very low temperatures. The contact resistance shows a slight increase with decreasing temperature which might originate from lower carrier energy leading to a lower probability of tunnelling through the barrier.

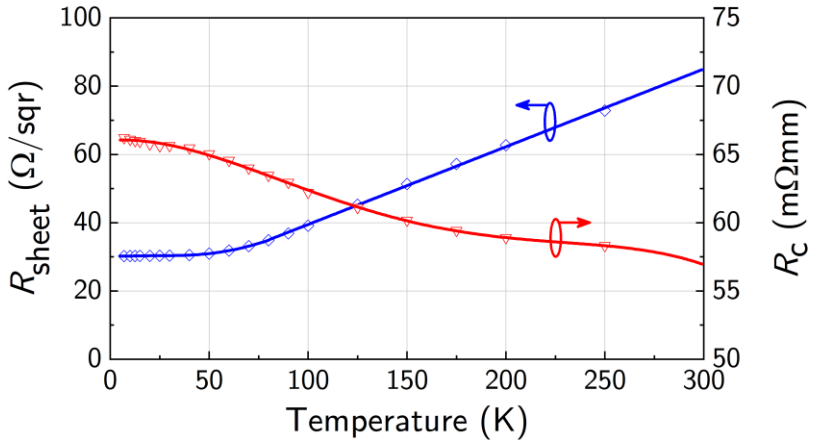
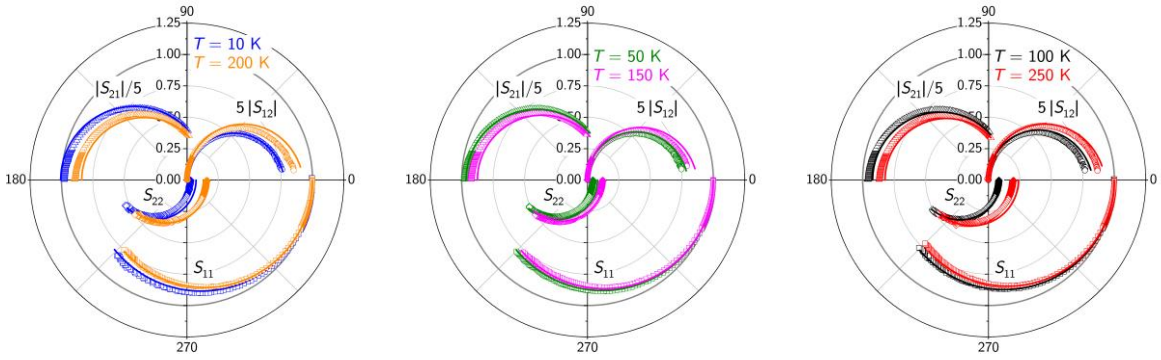


Figure 32: Measured (symbols) and modelled (lines) sheet resistance (blue) and contact resistance (red) dependent on the temperature.

The extrinsic capacitances show a slight increase at lower temperatures which is believed to be caused by thermal contraction in combination with a change in effective permittivity of the materials. The inductive elements are modelled temperature independent, since they are mainly dependent on the geometry, which does not change significantly during cooling [41].

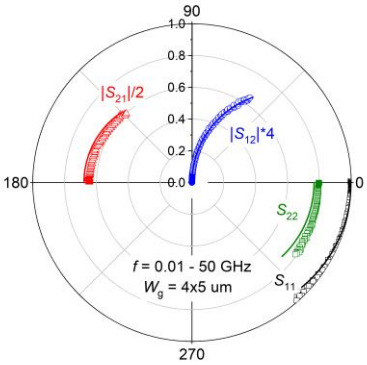
Besides the linear scaling with the unit gate width, the intrinsic elements are modelled bias and temperature dependent. This is implemented by a first to third order Taylor series (depending on the parameter) dependent on drain voltage, drain current and temperature. The coefficients are extracted using a dedicated simplex algorithm to minimize the root-mean-square deviation between a large set of on-wafer S-parameter measurements at various bias points and temperatures. This yields a fully bias, geometry and temperature scalable small-signal model. Figure 33 shows on-wafer S-parameter measurements and the corresponding model output of a 2 × 60 µm HEMT at several temperatures, which verifies the correct temperature dependent description of the small-signal parameters.



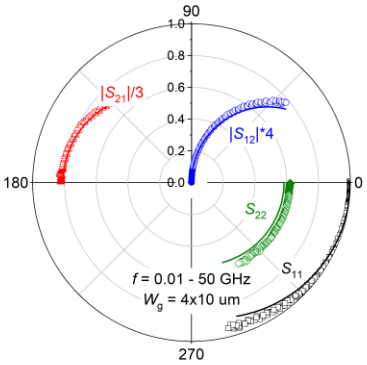
(a) (b) (c)

Figure 33: On-wafer measurements between 100 MHz and 50 GHz (symbols) and modelled (lines) S-parameters of common-source HEMTs with an absolute gate width of W_g *= 2 × 60 µm at* T *= 10 K (blue, (a)),* T *= 50 K (green, (b)),* T *= 100 K (black, (c)),* T *= 150 K (pink, (b)),* T *= 200 K (orange, (a)) and* T *= 250 K (red, (c)).*

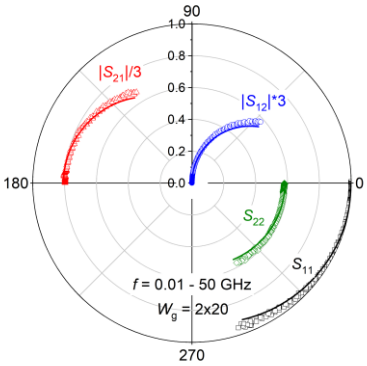
The model performance at cryogenic temperatures as deep as 10 K is of special importance since ultra-low-noise amplifiers for quantum computing or radio astronomy operate at this temperature. The scalability of the model at cryogenic conditions is demonstrated in Figure 34. On-wafer S-parameter measurements between 10 MHz and 50 GHz of very small and extremely large devices are predicted correctly by the model, proofing the high scalability at cryogenic temperatures.



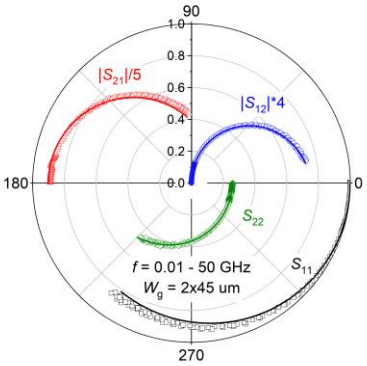
(a) W_g = 4 × 5 µm



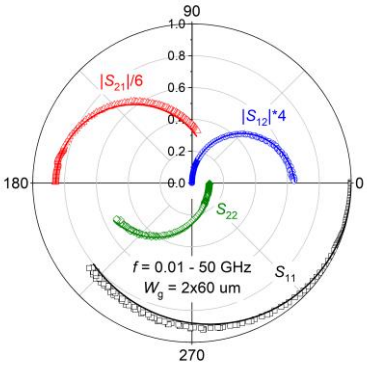
(b) W_g = 4 × 10 µm



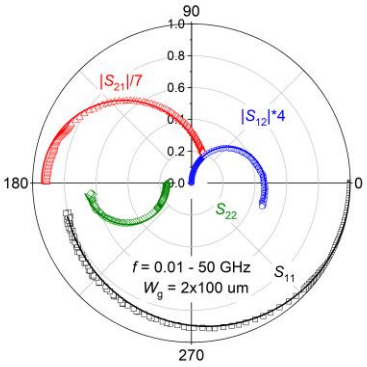
(c) W_g = 2 × 20 µm



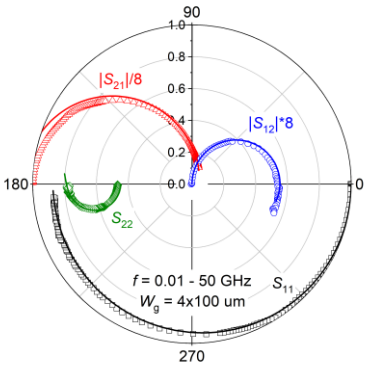
(d) W_g = 2 × 45 µm



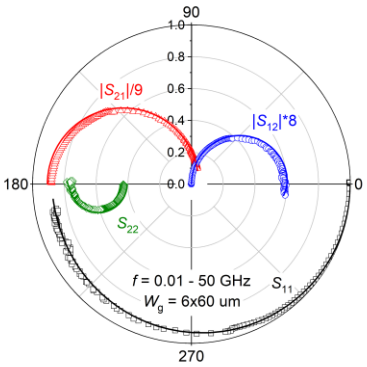
(e) W_g = 2 × 60 µm



(f) W_g = 2 × 100 µm



(g) W_g = 4 × 100 µm



(h) W_g = 6 × 60 µm

Figure 34: On-wafer measurements between 100 MHz and 50 GHz (symbols) and modelled (lines) S-parameters of common-source HEMTs with an absolute gate width (given in the above captions) at T = 10 K biased at V_d = 0.5 V, I_d = 50 mA/mm. Black: S_{11}, blue: S_{12}, red: S_{21}, green: S_{22}.

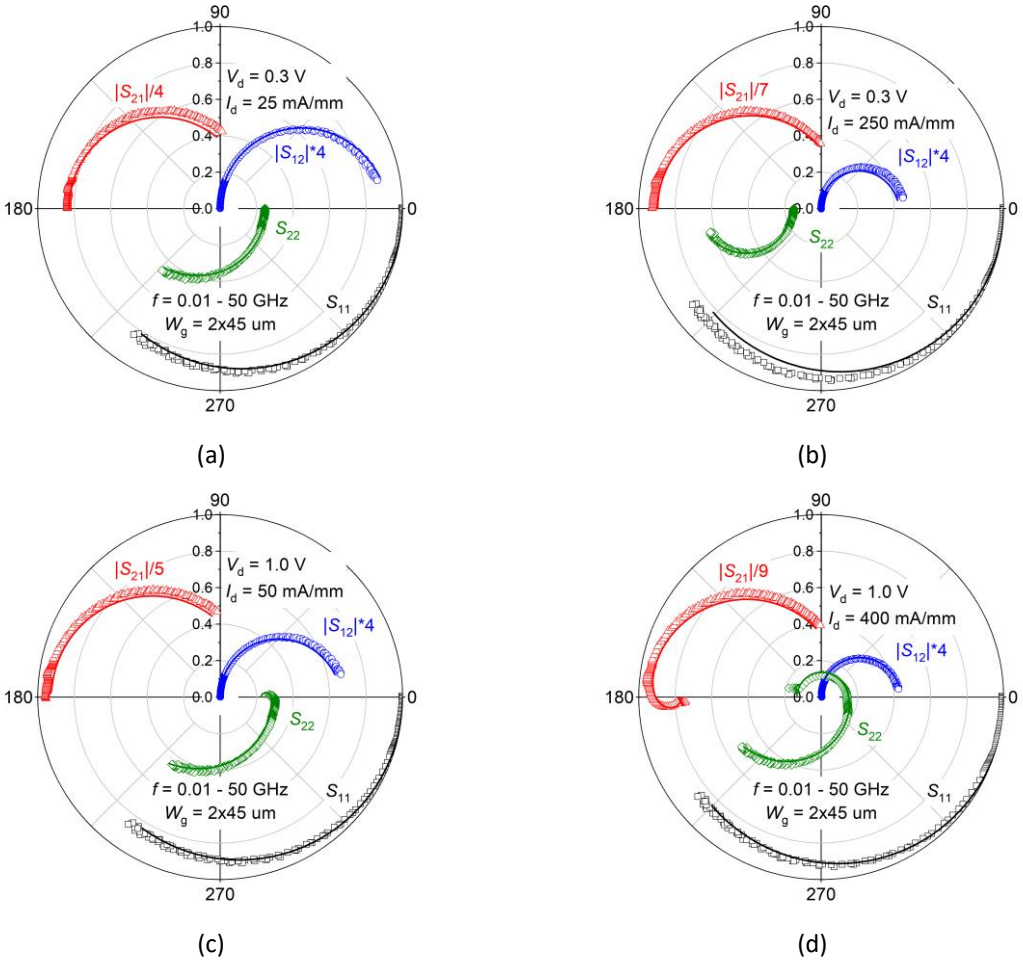


Figure 35: On-wafer measurements between 100 MHz and 50 GHz (symbols) and modelled (lines) S-parameters of a common-source HEMT with an absolute gate width of W_g = 2 × 45 µm at 10 K biased at V_d = 0.3 V, I_d = 25 mA/mm (a), V_d = 0.3 V, I_d = 250 mA/mm (b), V_d = 1 V, I_d = 50 mA/mm (c) and V_d = 1 V, I_d = 400 mA/mm (d). . Black: S_{11}, blue: S_{12}, red: S_{21}, green: S_{22}.

The coverage of a wide bias range at cryogenic temperatures is demonstrated in Figure 35 where S-parameter measurements of a 2 × 45 µm HEMT at 10 K in different bias points are compared with the model output. The model reproduces extreme bias points including very low current and very low voltage bias as well as very high current and voltage bias correctly. Therefore, the model can be used in arbitrary bias points at cryogenic conditions.

Measurements at cryogenic conditions are at IAF at the moment only possible up to 50 GHz, but the model is able to correctly reproduce room temperature measurements up to at least 150 GHz. Since the principle model-topology is the same for both cases and the equivalent circuit elements are frequency independent, it can be assumed that the cryogenic model is able to cover a comparably broad frequency range as the room temperature model.

The model demonstrates high scalability, wide coverage of bias points and high model accuracy over a very broad frequency range. Furthermore, all of the mentioned features are achieved at arbitrary temperatures between 10 K and 300 K. An accurate small-signal model forms the basis for almost every noise model. The excellent model characteristics make the proposed distributed model an excellent candidate for the inclusion of a scalable and temperature dependent noise model. The next modelling task is the extraction of a noise model both at room temperature and at cryogenic conditions based on the presented temperature dependent small-signal model.

5 Temperature-dependent device modelling and compact model development for III-V nanowire MOSFETs

Transistors developed at Lund University (ULUND) are based on III-V compound semiconductor nanowire channels, specifically vertical InAs/ InGaAs n-MOSFETs [42], [43], [44] and InAs/ InGaAsSb n-TFETs [45], [46]. Note that both device types utilise heterojunction channel engineering to boost device performance. The vertical MOSFETs have demonstrated up to 3.1 mS/µm transconductance, which is the highest transconductance reported for any transistor on a silicon substrate. The vertical TFETs were in the vanguard at demonstrating sub-60 mV/dec subthreshold swings at room temperature; reporting transfer characteristic swings as low as 31 mV/dec.

The thin nanowire channels, typically below 30 nm diameter depending on process and trimmed by digital etching, can yield prominent quantisation of the channel. A limited number of 1D sub-bands contribute to conduct the drain current of the transistor, depending on bias and temperature. This will contribute to an increased effective bandgap and a staircase-like transfer characteristic at low temperature. Physical models adapted at ULUND primarily rely on descriptions of quantisation, non-parabolicity, and quasi-ballistic transport in the narrow channel of the III-V MOSFET [47]. Temperature dependence enters naturally in the physical calculations but is currently not thoroughly described in the compact large signal models, especially w.r.t discrete sub-band conduction. The benefit of nanowire channels with gate all-around (GAA) is that equivalent gate control can be achieved at relaxed channel dimensions, as compared to planar devices. This reduces scattering and allows operation close to the ballistic limit at scaled channel lengths. Quasi-ballistic operation of short-channel devices is described based on Landauer's formulation and transmission coefficient for the MOSFET. However, a GAA device must be carefully designed to not introduce excess capacitance, which would limit the high frequency performance and prevent deployment in analogue/ mixed applications.

The large signal compact models currently adapted for ULUND devices are implemented in Verilog-A code. The models have primarily been validated towards data measured at room temperature where the effects of channel quantisation are limited. A simplification used is to describe the channel with one single effective sub-band, dominated by the actual sub-bands with lowest energy. The MOSFETs are described by an in-house Verilog-A model adapted based on the virtual source description, in conjunction with established transport and capacitance models [48], [49]. The TFET model is based on an open Verilog-A adaptation (T. Ytterdal at NTNU Trondheim, Norway), but reworked for nanowires, that describes the charge transport and partitioning [50], [51]. An overview of the models implemented for these two device types is presented below.

5.1 Modelling InGaAs Nanowire MOSFETs on Silicon

The vertical InAs/ InGaAs nanowire MOSFET is fabricated on a silicon substrate padded with an InAs buffer layer. This buffer layer serves as source mesa and the InAs nanowire core is grown graded and overgrown with InGaAs. This provides a graded InGaAs drain region for the device. Lifting layer dielectrics, high-k gate dielectric, and sputtered metals are defined to form the final device. One key feature of the gate last device process is the inherent ability to self-align the gate electrode with respect to the drain contact [42].

Measured transfer and output current-voltage (IV) characteristics of a vertical InAs/ InGaAs nanowire MOSFET are presented in Figure 36, characterized at room temperature. The response of the fitted large signal virtual source (VS) model, described in the following, is also shown. It can be noted that the model is in close agreement with the measured data both for transfer and output characteristics and over the reported range.

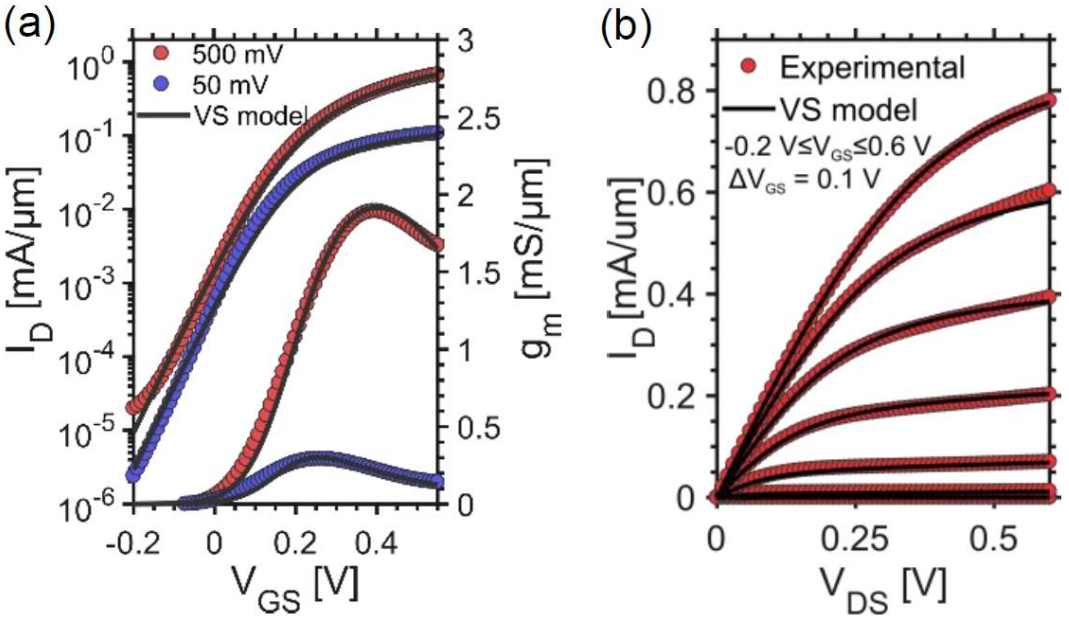


Figure 36: Measured IV characteristics of the n-MOSFET developed at ULUND with fitted virtual source (VS) large signal model, from [43].

The implemented virtual source (VS) model allows for a current-voltage description based on a top of the barrier, a.k.a virtual source located at $x = x_0$, description in the MOSFET [48]. Use of the charge-sheet approximation yields the drain current,

$$I_D = Q_{ix_0} v_{x_0} F_s, \tag{30}$$

from the charge density Q_{ix_0}, effective charge carrier velocity v_{x_0}, and F_s denotes the saturation function. The carrier velocity is the effective thermal velocity for a short channel device. This can also be treated as the unidirectional thermal velocity modified by the transmission coefficient in a quasi-ballistic device. The saturation function,

$$F_s = \frac{V_{DS}/V_{sat}}{\left(1+[V_{DS}/V_{sat}]^{\beta}\right)^{1/\beta}}, \tag{31}$$

achieves stitching of the linear and saturation region of operation, where V_{sat} denotes the saturation voltage and β is a shaping parameter with a typical value of about 1.8.

The model also adapts a charge partitioning model for the description of capacitances [49], validated based on RF measurements and small-signal modelling.

5.2 Modelling InGaAsSb TFETs on Silicon

The vertical InAs/ InGaAsSb heterojunction nanowire n-TFETs are fabricated on a silicon substrate padded with an InAs buffer layer. This buffer layer serves as drain mesa and the InAs nanowire core is grown and switched to GaSb to form the tunnel junction, but an InGaAsSb source segment is formed in between due to a memory effect in the nanowire growth. This provides a tunnel junction from an InGaAsSb source region to an InAs drain, with contacts formed on the GaSb top and InAs mesa, respectively. Lifting layer dielectrics, high-k gate dielectric, and sputtered metals are defined to form the final device [45].

Measured transfer and output current-voltage (IV) characteristics of a vertical InAs/ InGaAsSb nanowire TFET are presented in Figure 37, characterized at room temperature. The response of the fitted large signal NTNU model, described below, is also shown. It can be noted that the model is in good agreement with the measured data.

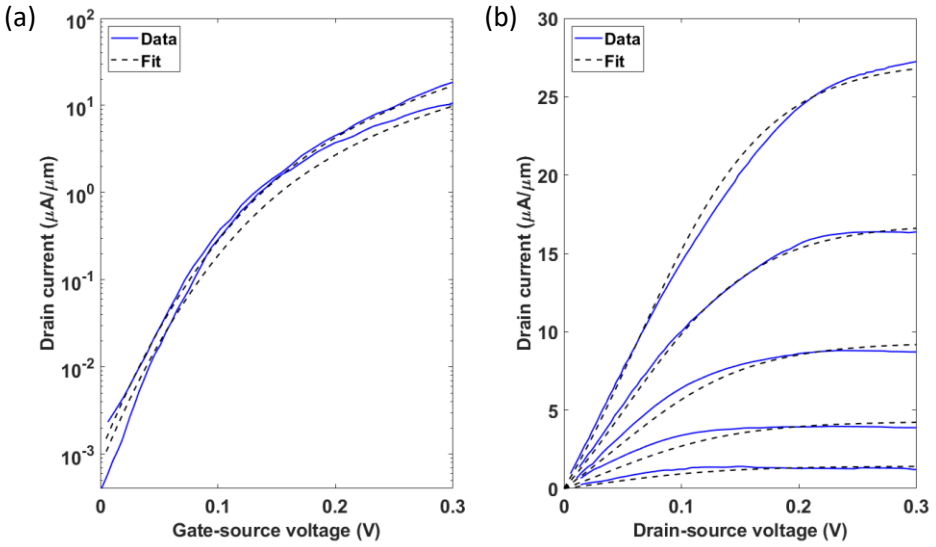


Figure 37: Measured IV characteristics of the n-TFET developed at ULUND with fitted NTNU large signal model, based on [45].

The adapted model is implemented from an analytic description of a generalised TFET based on the Kane-Sze formula [50]. The modified Kane-Sze expression yields the drain current,

$$I_D = afV_{TW}\xi \exp\left(-\frac{b}{\xi}\right), \tag{32}$$

where a and b are related to the material properties of the tunnel junction, V_{TW} denotes the tunnelling window in volts, f is a dimensionless factor that describes current onset and saturation w.r.t. V_{DS}, and ξ estimates the maximum electric field in the tunnelling junction. It should be noted that the tunnelling window decays exponentially w.r.t. V_{GS} outside direct overlap due to band tails, which can be described via the Urbach parameter. The above expression is valid in the first quadrant and is complemented by additional expressions that describe the ambipolar, diode, and negative differential resistance regions of operation.

The capacitive characteristics of the TFET are adapted from RF measurements [46]. Capacitances are currently implemented as linear fits to measured data and should be revised in future works based on device physics [50], [51].

6 Summary and conclusions

This report presented the progress made in WP2 on the modelling of various devices at room and at cryogenic temperatures.

The first Section EPFL presented the simplified EKV MOSFET model and how it can be used to characterize MOSFETs operating at room temperature but also at cryogenic temperatures. The important notion of inversion coefficient is introduced and it is shown how it can be used to describe the device operation from weak to strong inversion. The model can be used to express various figures-of-merit such as the current efficiency G_m/I_D in terms of the inversion coefficient requiring only a single parameter, namely the velocity saturation parameter λ_c. The later FoM has been measured at cryogenic temperature for both bulk and FDSOI CMOS technologies and it is shown that it is almost invariable to technology and to temperature. Another FoM is the transit frequency which can also be expressed in terms of the inversion coefficient. The later has not yet been measured at cryogenic temperature, but since it strongly depends on the transconductance there is a good chance that the normalized FoM will fit the model even at cryogenic temperature. Since the simplified EKV model only requires 4 parameters (5 for FDSOI), it can be useful for designers to better size and select the optimum operating point, while waiting for the compact models that are available in PDKs to be accurate enough at cryogenic temperatures. The extraction of these 4 parameters can be quite cumbersome. For this reason, a fully automated parameter extraction tool based on Python has been developed and validated on 22 nm FDSOI devices at room and cryogenic temperatures. This tool is made available to the consortium and work is on-going to make it accessible on a dedicated web-site.

INPG and LETI have demonstrated Poisson-Schrödinger simulations and an analytical charge model for a back biased FDSOI structure operated at deep cryogenic temperatures. Moreover, PS simulation has even been conducted down to 0K, where metallic statistics applies, by replacing the F_0 Fermi integral by a Heaviside function. Considering, as a first approximation, two separated channels for front and back interface, INPG and LETI have established a set of analytical equations based on a single subband scheme within an Airy's function approach, providing a good description of the surface potential, the inversion charge and the capacitance characteristics of FDSOI structures operated at very low temperature and for various back bias and silicon thickness. This analytical charge model is a first step towards a cryogenic compact model for FDSOI MOSFET with back biasing action, which will be transferred to UTSOI LETI platform in the near future.

Fraunhofer IAF has presented a temperature dependent distributed small-signal modelling approach that has been demonstrated at IAF's 50 nm mHEMT technology. The high scalability in terms of transistor geometry (gate-width, finger number) of the distributed approach has been demonstrated at on-wafer S-parameter measurements of HEMTs with high absolute gate width and devices with very small absolute gate width. The model is able to correctly reproduce the measurements up to at least 150 GHz, validating its broadband frequency response. All bias points that are typically applied to HEMTs are correctly described, including extremely low current and voltage bias as it is used in typical cryogenic LNAs. Furthermore, all this excellent model features are available at arbitrary temperatures between 10 K and 300 K. This is achieved by precise modeling of the temperature dependency of the various equivalent circuit elements building the model. The excellent model characteristics make the proposed distributed model an excellent candidate for the inclusion of a scalable and temperature dependent noise model, which will be the next modelling task.

The results from ULUND indicate the starting point of the large signal compact device modelling effort for III-V nanowire MOSFETs and TFETs. These models will be developed further in SEQUENCE. Estab-

lished modelling approaches such as the VS and the NTNU code are augmented with physical parameters and geometrical scaling, then fitted to measured data. The data fitting support is primarily IV characteristics and small signal RF scattering parameters. Device variability is typically non-negligible in a batch-batch perspective, which poses challenges in the validation. However, the models fit well to devices from the same batch and can be used for approximate prediction of circuit performance. Future studies will focus on refined descriptions of the temperature dependence. This can be better described based on physical considerations of the devices. The models will also be revised and updated based on any recent advancements in the field. Systematic validation based on complementary measurement techniques will also be critical.

7 References

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